TEKER TORRES & TEKER, P.C.
SUITE 2A, 130 ASPINALL AVENUE
HAGÅTÑA, GUAM 96910
TELEPHONE: (671) 477-9891/4
FACSIMILE: (671) 472-2601
Attorneys for Plaintiffs
Nanya Technology Corp. and
Nanya Technology Corp. U.S.A.

FILED
DISTRICT COURT OF GUAM

JUN 26 2007

MARY L.M. MORAN
CLERK OF COURT

IN THE DISTRICT COURT OF GUAM

NANYA TECHNOLOGY CORP. and NANYA TECHNOLOGY CORP. U.S.A. Plaintiffs, vs. FUJITSU LIMITED and FUJITSU MICROELECTRONICS AMERICA, INC. Defendants.	CIVIL CASE NO. 06-CV-00025 **PLAINTIFFS' SUR-REPLY IN OPPOSITION TO FUJITSU LIMITED'S REPLY IN SUPPORT OF ITS MOTION TO DISMISS OR TRANSFER**

I.   NANYA'S EVIDENCE REQUIRES DENIAL OF THE MOTION TO DISMISS

In its Reply, Fujitsu Limited ("Fujitsu") strategically ignores 35 U.S.C. § 271, which specifically provides that "whoever without authority makes, uses, offers to sell, or sells any patented invention, within the United States, or imports into the United States any patented invention during the term of the patent therefore, infringes the patent." As the admitted ***manufacturer*** of the accused microcontroller and memory devices and head of the global Electronic Devices Group (a group that includes FMA), Fujitsu tellingly fails to deny that its accused microcontroller and memory devices are injected into and sold through extensive national distribution networks that reach the entire U.S., including Guam.

Contrary to Fujitsu's claim that it sells "no products on the island of Guam," Nanya has obtained compelling evidence that Fujitsu's accused devices are regularly sold on Guam through customary distribution channels.[1] Game consoles such as the Nintendo DS Lite,[2] and possibly the Sony PlayStation Portable,[3] contain the accused memory devices and are commonly sold on Guam to Guam consumers.

---

[1] *See* Exhibits 29, 40-42, and 56 of Plaintiffs' Response and Memorandum in Opposition to Defendants' Motion to Dismiss or Transfer to the Northern District of California ("Response") [Dkt. No. 254].
[2] *See* Exhibit M, Declaration of Joseph C. Razzano in Support of Plaintiffs' Sur-Reply to Defendant's Motion to Dismiss ("Razzano Decl.") [Dkt. No. 297], ¶5; Exhibit N, Declaration of Santos Garza, Ph.D., P.E. ("Garza Decl."), ¶3; Exhibit P, Declaration of Peter Duane Cruz ("Cruz Decl.") [Dkt. No. 298], ¶¶3, 5-6; Exhibit O, Declaration of Andrew Huffstetler ("Huffstetler Decl."), ¶¶9-13; Exhibit C, Materials related to Fujitsu device MB82DBS02163C found in Nintendo DS Lite game console; Exhibit T, Materials related to business relationship between nVidia/Nintendo and Fujitsu.
[3] *See* Razzano Decl. at ¶8; Cruz Decl. at ¶¶4, 6; Huffstetler Decl. at ¶¶14-17. Exhibit B, Materials related to device MB44C012 found in

Moreover, Fujitsu's products are available for direct purchase on Guam.[4] Fujitsu computer hard-drives have been purchased by employees of the University of Guam[5]; Fujitsu laptops are commercially available to Guam professionals[6] and a computer store in Tamuning sells Fujitsu computer batteries.[7] Such sales evidence Fujitsu's regular and purposeful contacts with Guam.

In its Response, Nanya also presented the Court with uncontroverted evidence[8] that: (1) actual sales of the accused devices regularly occur on Guam; (2) the accused devices are incorporated in products sold or offered for sale on Guam; and (3) Fujitsu had offered to sell the accused devices to customers without restriction throughout the U.S., including Guam. Placement of infringing products in the stream of commerce is a well-recognized basis for jurisdiction.[9] Fujitsu cannot credibly bury its head in the sand and offer the excuse that its products are not available throughout Guam because "my distributor did it." Indeed, numerous cases find jurisdiction based upon the unrestricted sale of an accused product to a "nationwide" distributor.[10]

The evidence establishes that the accused devices – manufactured by Fujitsu and sold by FMA – are in many of the automobiles commercially available on Guam. Nanya has submitted indisputable evidence that the Toyota Prius automobile – sold on Guam for the past several years – contains at least one of the accused microcontroller devices.[11] And Fujitsu's other numerous "design wins" demonstrate that it purposefully designs and manufactures the accused devices for incorporation into BMW,[12] GM,

---

Sony PSP game console. The evidence demonstrates Fujitsu's business relationship with Sony. *See* Exhibit 25 of Response, spreadsheet records listing customers for Fujitsu devices (Sony); *See* Exhibit 28 of Response, order confirmation for Sony Ste Support Center; *see* Exhibit 28 of Response, Fujitsu Standard Analysis reports regarding sales of multiple devices to multiple entities ("Sony Elec." and "Sony Ste."). Neither Fujitsu Ltd. nor FMA produced documents regarding this device despite its clear relevance to Nanya's discovery requests. Because of Defendants' failure to produce documents related to this device, Nanya needs further discovery from Defendants to be able to confirm whether this device infringes Nanya's patents. Nanya's discovery of this device and others found in products on Guam and Defendants' failure to produce documents related to these devices clearly establish that Defendants are withholding key documents on the sale and use of their accused products in the U.S.

[4] Contrary to Fujitsu's allegations, these were not "manufactured" sales for the purpose of establishing jurisdiction but ordinary sales made in the ordinary course of business that confirm the presence of infringing devices on Guam before suit was filed.

[5] *See* Exhibit 41 of Response, University of Guam invoice for a Fujitsu hard drive.

[6] *See* Exhibit 40 of Response, Purchase materials related to purchase of Fujitsu laptop computer.

[7] *See* Exhibit 42 of Response, Receipt for purchase of Fujitsu lithium ion computer battery.

[8] As the Court is aware, Fujitsu has blocked Nanya's efforts at discovery, not only producing approximately 800,000 pages of documents after the depositions, but, equally important, refusing to provide designated corporate representatives to testify on behalf of Fujitsu or FMA. The deposed witnesses were not willing or able to testify on behalf of Fujitsu or FMA; they only testified to their own knowledge and hearsay "beliefs" garnered from others. *See* Exhibit E, Deposition transcript of Shigeru Kitano, pages 18-19, 26, 35-36, 38-39, and 46-48. If Defendants had not stonewalled in jurisdictional discovery, the jurisdictional issues would be simple – because the accused devices are awash in Guam.

[9] *Maxwell Chase Tech., L.L.C. v. KMB Produce, Inc.*, 79 F.Supp.2d 1364, 1367 (N.D.Ga., 1999); *Motorola, Inc. v. PC-Tel, Inc.*, 58 F. Supp.2d 349, 353 (D.Del., 1999).

[10] *See, e.g., Motorola, Inc. v. PC-Tel, Inc.*, 58 F.Supp.2d at 353; *Maxwell Chase Tech.*, 79 F.Supp 2d at 1371-72.

[11] *See* Razzano Decl. at ¶10; Exhibit Q, Declaration of David Carey ("Carey Decl."), Exhibit B, and pp. 31 and 42; Huffstetler Decl. at ¶¶3-8. Exhibit F, Materials related to accused Fujitsu microcontroller device MB90583C found in the Toyota Prius automobile; Exhibit G, Materials demonstrating Fujitsu's business relationship with Toyota as a direct customer and as an end customer. Exhibit U, Declaration of Steven L. Aguon.

[12] Despite representing at the June 20, 2007 Hearing that one of the accused devices would not be present in BMW automobiles until 2008, there is evidence demonstrating that Fujitsu's sales of various accused devices to parts suppliers to be incorporated into BMW automobiles in the past several years. *See* Exhibit H, Materials evidencing various accused devices being sold or offered for sale to be incorporated into

Toyota, Land Rover,[13] and Ford[14] automobiles (all of which are offered for sale on Guam). Further, Fujitsu's marketing materials list numerous automotive parts suppliers[15] as conduits to ultimately distribute the accused devices in these companies' automotive applications. Finally, GE, Xerox, Source Medical,[16] and Whirlpool are all listed as marketing targets for consumer applications for various accused devices.[17] By targeting these companies – all of whom have nationwide distribution networks – as means for distribution of its accused devices, it is beyond cavil that Fujitsu (with assistance of FMA) knowingly distributes its accused devices throughout the U.S.

Contrary to Fujitsu's unsubstantiated allegations, Nanya has specifically identified the accused products as "MCU" and "microcontroller" devices and provided an exemplary list of model and parts numbers.[18] The evidence irrefutably demonstrates that the accused devices are directly sold or offered for sale on Guam and that they are incorporated into products found throughout the U.S., including Guam.[19] Specifically, Fujitsu:

- ***does not deny*** that it manufactures and offers to sell the accused devices to customers with national distribution networks without restriction;
- ***does not deny*** that the accused devices are designed to be incorporated into a variety of applications, including automotive and consumer electronic applications.
- ***does not deny*** that the accused devices are incorporated into products such as Toyota, GM, and Ford automobiles; Olympus and Canon[20] digital cameras; Nintendo game consoles; and Lexar and SanDisk memory devices.
- ***does not deny*** that such products were purchased and are available for purchase on Guam.

Though Fujitsu attempts to ignore these facts, it would be error for this Court to do so. The *Donnelly Corp.* case is particularly instructive.[21] There, a foreign defendant sold infringing automotive

---

BMW automobiles.

[13] *See* Exhibit S, Document states that Land Rover is using Fujitsu's Jade GDC and is supported by FMA. *See* FMA_0034212.

[14] *See* Exhibit I, Documents that describe North America Automotive Projects and list several accused microcontroller devices incorporated into Ford automobiles through parts suppliers Denso and Delphi.

[15] *See* Exhibit D, Eastern Area MCU Update, FMA_0133639.

[16] *See* Exhibit J, Press release showing that Fujitsu Ltd. provides computers and information management solutions to Source Medical, a provider of outpatient information solutions, with products installed in over 3500 ambulatory surgery centers, surgical hospitals and other health care practices throughout the U.S. The release ***specifically includes Guam***.

[17] *See* Exhibit D , Eastern Area MCU Update at FMA_0133640-641.

[18] *See* Chart, attached hereto as Exhibit K. Fujitsu's additional argument that the pleading is insufficient is entirely baseless. Case law and Federal Rule 8(a) expressly provide that a patent pleading is sufficient if it places the alleged infringer "on notice" and ensures that the accused infringer "has sufficient knowledge of the facts alleged to enable it to answer the complaint and defend itself." *See Meridian Enterprises Corp. v. Bank of America Corp.*, No. 4:06CV01117 RWS, slip op. at 1, 2006 WL 3210497 (E.D. Mo. Nov. 3, 2006) ("[A] patentee need only plead facts sufficient to place the alleged infringer on notice. This requirement ensures that an accused infringer has sufficient knowledge of the facts alleged to enable it to answer the complaint and defend itself"); *Nichia Corp. v. Seoul Semiconductor Ltd.*, No. C-06-0162-MMC, 2006 WL 1233148, 1 (N.D. Cal. May 9, 2006).

[19] Ironically, one of Fujitsu's declarations disavows and "corrects" statements made in Fujitsu's own self-serving advertisements. The entire Declaration of Akio Nezu consists of "correcting" an alleged advertising mistake that marketed the accused microcontroller device as compatible for blood glucose monitors. Fujitsu's argument stills fails as the advertisement represents an offer to sell the accused microcontroller device, thus subjecting Fujitsu to liability. *See* Fujitsu Limited's Reply In Support of Its Motion to Dismiss [Dkt. No. 264].

[20] *See* Exhibit R, Document lists Canon as one of EDG's Top Ten Worldwide Customers of which FMA is part of EDG.

[21] *Donnelly Corp. v. Reitter & Schefenacker GmbH & Co. KG*, 189 F. Supp. 2d 696, 708 (W.D. Mich. 2002){ TA \l "*Donnelly Corp. v. Reitter & Schefenacker GmbH & Co. KG*, 189 F. Supp. 2d 696, 708 (W.D. Mich. 2002)" \s "Donnelly" \c 1 }.

---

mirrors through a worldwide distribution network to manufacturers who incorporated the infringing mirrors into products eventually sold in the U.S., including the forum. The *Donnelly* court imposed personal jurisdiction, stating that because the automotive mirrors "landed in Michigan through 'the regular and anticipated flow of products, Defendant had to expect suits in the U.S. arising out of its sale of the mirrors, given that it directed the mirrors to American markets."[22] Similarly, Fujitsu directs its microcontroller devices to U.S. markets by selling them through a worldwide distribution network to manufacturers who incorporate them into products sold in the U.S., including the forum. Because the accused microcontroller devices arrive in Guam through the regular flow of commerce, Fujitsu must anticipate suit anywhere the accused devices are found, including Guam.

II. FUJITSU FAILS TO REBUT JURISDICTION UNDER THE CLAYTON ACT

Fujitsu does not deny that jurisdiction is proper over it under the Clayton Act. Instead, Fujitsu attempts to escape personal jurisdiction under Section 12 of the Clayton Act by improperly focusing on a defendant's "presence" in the forum state. To the contrary, Clayton Act jurisdiction focuses on the anticompetitive acts of the defendant and whether the anticompetitive effect of that conduct reaches the forum. It is indisputable that Fujitsu's anticompetitive conduct will have an effect wherever its and its competitors' products are sold, namely, throughout the United States.

Additionally, Fujitsu improperly conflates personal jurisdiction and venue.[23] Fujitsu ignores that the Ninth Circuit has held that determination of the sufficiency of service of process on the one hand and the determination of venue under Section 12 of the Clayton Act should be analyzed ***separately***.[24] Section 12 provides that a party may properly effect service worldwide, ***but does not designate actions for effecting service***. Rather, plaintiffs are to serve defendants under Rule 4 of the Federal Rules of Civil Procedure or pursuant to an applicable treaty such as the Hague Convention.[25] Nanya properly served Fujitsu in accordance with Section 12 of the Clayton Act and the applicable Rule 4.

---

[22] *Id.*

[23] Fujitsu has no authority for its argument and merely attempts to rely on a case that has no precedential value in this Court. Indeed, the Eleventh Circuit court merely analyzed Section 12 of the Clayton Act in concurrence with the federal rules for service of process. *See General Cigar Holdings, Inc. v. Altadis, S.A.*, 205 F.Supp.2d 1335, 1340 (S.D.Fla. 2002).

[24] *See Action Embroidery Corp. v. Atlantic Embroidery, Inc.*, 368 F.3d 1174, 1180 (9th Cir. 2004) ("[E]xistence of personal jurisdiction over an antitrust defendant does not depend upon there being proper venue in that court."); *see also Go-Video, Inc. v. Akai Electric Co. Ltd.*, 885 F.2d 1406, 1414 (9th Cir.1989) (holding that because §12 allows for service of process anywhere in the country and because venue under §1391(d) is proper in any judicial district, personal jurisdiction for an antitrust suit against a foreign corporation is proper in any judicial district in the United States).

[25] *See Dee-K Enterprises, Inc. v. Heveafil Sdn. Bhd.*, 982 F.Supp. 1138, 1144 (E.D.Va. 1997) (stating that the requirements for service of process are "met both by §12 of the Clayton Act, 15 U.S.C. § 22, and by Rule 4(k)(2). Section 12 provides for nationwide-indeed worldwide-service of process when antitrust defendant is a corporation.").

Because this Court has personal jurisdiction over Fujitsu with respect to Nanya's Clayton Act claims, this Court also has pendent personal jurisdiction over Fujitsu for both Nanya's Sherman Act claims and the patent claims.[26] A federal court has agreed that when antitrust claims and patent claims "derive from a common nucleus of operative fact" then jurisdiction over both claims pursuant to the doctrine of pendent personal jurisdiction is proper.[27] Nanya's Sherman Act claims and patent claims all relate to the same common nucleus of operative facts – Fujitsu's illegal demands made in licensing negotiations. Pricing and competitive conduct are fundamentally related to manufacture and sales.[28] Moreover, the fact that Fujitsu's patents are invalid is the basis of Nanya's claims regarding Fujitsu's anticompetitive conduct. Fujitsu cannot gloss over the interrelated nature of the Clayton Act, Sherman Act, and patent claims with conclusory statements. Because this Court has jurisdiction over the Clayton Act claims and discretion to resolve the patent and declaratory judgment claims, dismissing any of Nanya's claims would only promote piecemeal litigation and waste judicial resources.

III.   FUJITSU FAILS TO SHOW CALIFORNIA IS A MORE CONVENIENT VENUE THAN GUAM[29]

Fujitsu argues that because Nanya did not file in its "home base," Nanya's choice of venue should be afforded minimal to no deference. Unlike other disputes (such as the *Sinochem*[30] case), Nanya cannot file in its "home base" of Taiwan. Courts routinely hold in patent cases that: "While transfer of a case will generally be regarded as less inconvenient to a plaintiff if the plaintiff has not chosen its 'home turf' or a forum where the alleged wrongful activity occurred, the plaintiff's choice of forum is still of paramount consideration, and ***the burden remains at all times on the defendants to show that the balance of convenience and the interests of justice weigh strongly in favor of transfer.***"[31] In light of

---

[26] *Action Embroidery*, 368 F.3d at 1180-81 ("***Pendent personal jurisdiction is typically found where one or more federal claims*** for which there is nationwide personal jurisdiction are combined in the same suit with ***one*** or more state or ***federal claims*** for which there is not nationwide personal jurisdiction.") (emphasis added); *Miller Pipeline Corp. v. British Gas Plc*, 901 F.Supp. 1416, 1424 (S.D. Ind., 1995); *Robinson Eng'g. Co., Ltd. Pension Plan Trust v. George*, 223 F.3d 445, 449-450 (7th Cir. 2000); *ESAB Group, Inc. v. Centricut, Inc.*, 126 F.3d 617, 628-629 (4th Cir. 1997); *IUE AFL-CIO Pension Fund v. Herrmann*, 9 F.3d 1049, 1056-1057 (2d Cir. 1993); *Oetiker v. Werke*, 556 F.2d 1, 5 (D.C. Cir. 1977).

[27] *See Miller Pipeline Corp. v. British Gas plc*, 901 F.Supp. 1416, 1424 (S.D. Ind., 1995) ("This Court finds that personal jurisdiction exists over British Gas as to the antitrust claim pursuant to 15 U.S.C. § 22, and as to the patent claim pursuant to the doctrine of pendent personal jurisdiction.").

[28] The nature and extent of Fujitsu's sales and manufacturing activities relative to the entire market relate directly to whether its conduct is anticompetitive.

[29] Defendants' claim that the jurisdictional issues are complex is a red herring. What has been complex are Defendants' efforts to avoid jurisdictional discovery through the production of volumes of irrelevant documents and the non-production of the relatively few documents that they know demonstrate the Court's proper exercise of jurisdiction.

[30] *Sinochem Intern. Co. Ltd. v. Malaysia Intern. Shipping Corp.*, 127 U.S. 1184, 1189 (2007).

[31] *Critikon, Inc. v. Becton Dickinson Vascular Access, Inc.*, 821 F.Supp. 962, 965 (D. Del. 1993) (emphasis added).

the foregoing, Fujitsu's transfer request must also be denied.

Dated at Hagåtña, Guam on June 26, 2007

<div align="center">

TEKER TORRES & TEKER, P.C.

By: _____

JOSEPH C. RAZZANO, ESQ.

</div>

1 **TEKER TORRES & TEKER, P.C.**
   SUITE 2A, 130 ASPINALL AVENUE
2 HAGÅTÑA, GUAM 96910
   TELEPHONE: (671) 477-9891/4
3 FACSIMILE: (671) 472-2601

4 **UNPINGCO & ASSOCIATES, LLC**
   SUITE 12B, SINAJANA MALL
5 777 ROUTE 4, SINAJANA, GUAM
   671.475.8545 TELEPHONE
6 671.475.8550 FACSIMILE

7 **SHORE CHAN BRAGALONE LLP**
   SUITE 4450, REPUBLIC CENTER
8 325 N. ST. PAUL STREET
   DALLAS, TEXAS 75201
9 TELEPHONE: (214) 593-9110
   FACSIMILE: (214) 593-9111
10

11 *Attorneys for Plaintiffs.*

12

13

14

15   **IN THE DISTRICT COURT OF GUAM**

16

17 NANYA TECHNOLOGY CORP. AND   Case No. CV-06-00025
   NANYA TECHNOLOGY CORP. U.S.A.,
18   **APPENDIX IN SUPPORT OF**
                  Plaintiffs,   **PLAINTIFFS' SUR-REPLY IN**
19 v.   **OPPOSITION TO FUJITSU LIMITED'S**
                                         REPLY IN SUPPORT OF ITS MOTION
20 FUJITSU LIMITED AND FUJITSU   **TO DISMISS OR TRANSFER**
   MICROELECTRONICS AMERICA, INC.,
21   **FILED UNDER SEAL**
                  Defendants.
22

23

24

25

26

27

28   ORIGINAL

                            -1-

TABLE OF CONTENTS

* - All or a portion of exhibit is filed under seal

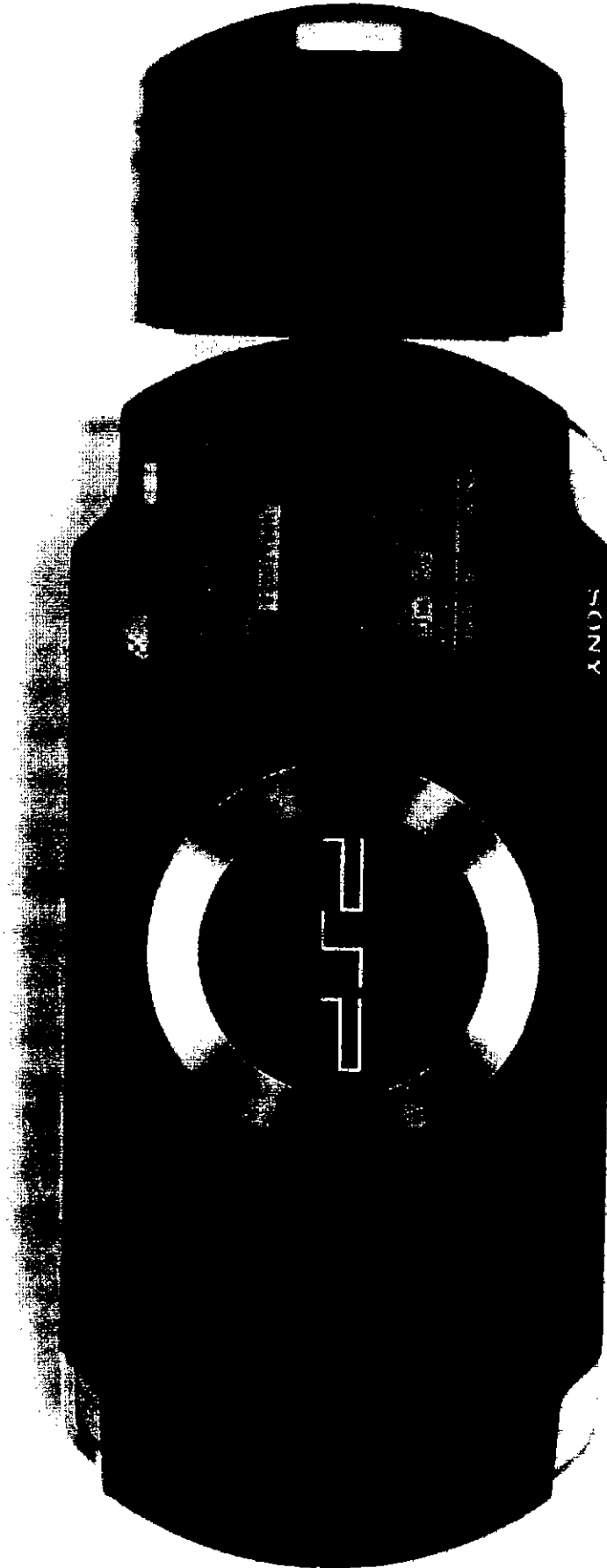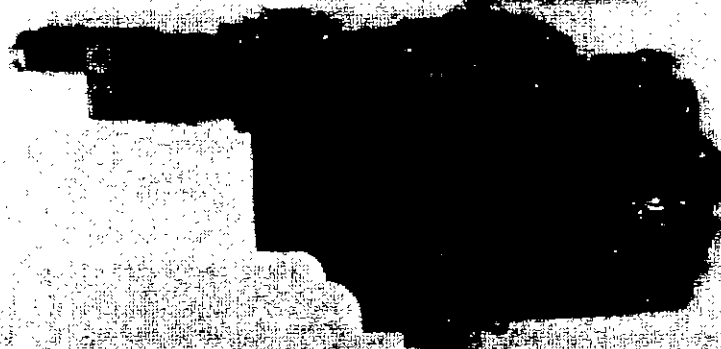| EXH. NO.	DESCRIPTION
B	Materials related to MCU device found in Sony PSP game console
C	*Materials related to MCU device found in Nintendo DS Lite game console
D	*Eastern Area MCU Update, FMA0133637-133644
E	*Deposition excerpts from the April 25, 2007 deposition of Shigeru Kitano
F	Materials related to MCU device found in the Toyota Prius automobile
G	*Materials related to Toyota's business relationship with Fujitsu
H	*Materials evidencing various MCU devices pertaining to BMW automobiles
I	*Materials evidencing various MCU devices pertaining to Ford automobiles
J	Source Medical article, "Fujitsu and Source Medical showcase pen-based outpatient information system"
K	Chart summarizing Nanya's evidence rebutting FJ's claims
L	Declaration of Martin Pascual
M	Declaration of Joseph Razzano
N	Declaration of Santos Garza
O	Declaration of Andrew Huffstedler
P	Declaration of Peter Cruz
Q	Declaration of David Carey
R	*Materials related to MCU device found in Canon cameras
S	*Materials related to MCU device pertaining to Land Rover automobile
T	*Materials related to NVidia/Nintendo's business relationship with Fujitsu
U	Declaration of Steven L. Aguon

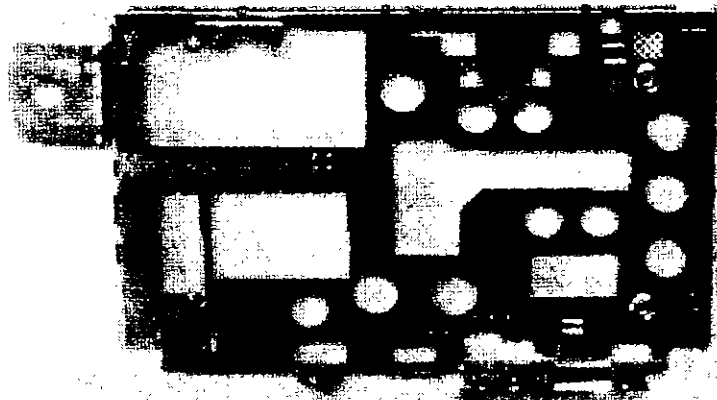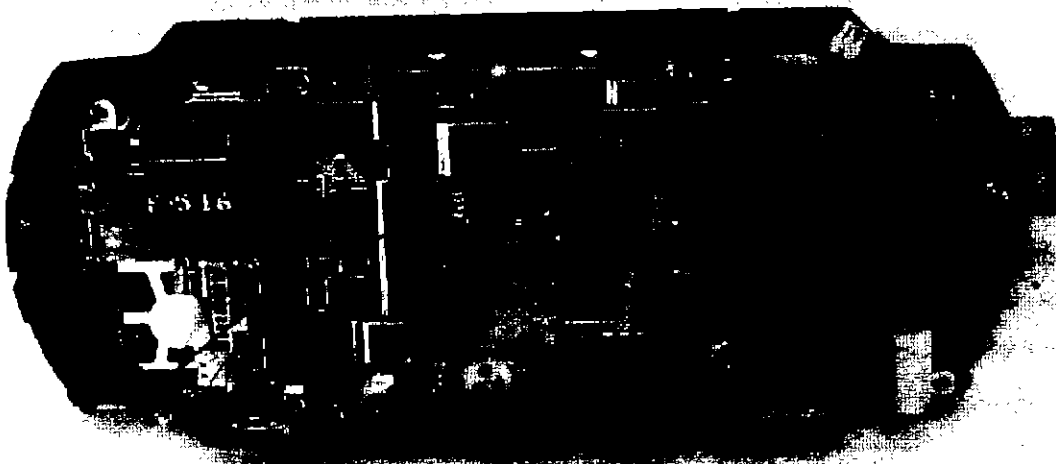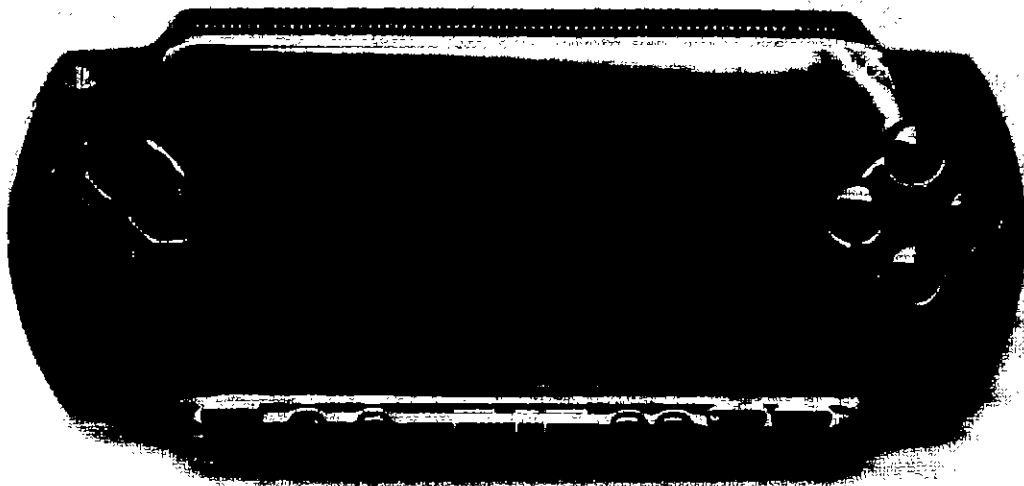Dated at Hagåtña, Guam on June 26, 2007   Respectfully submitted

TEKER TORRES & TEKER, P.C.

By:/s/ Joseph C. Razzano

JOSEPH C. RAZZANO, ESQ.

EXHIBIT B
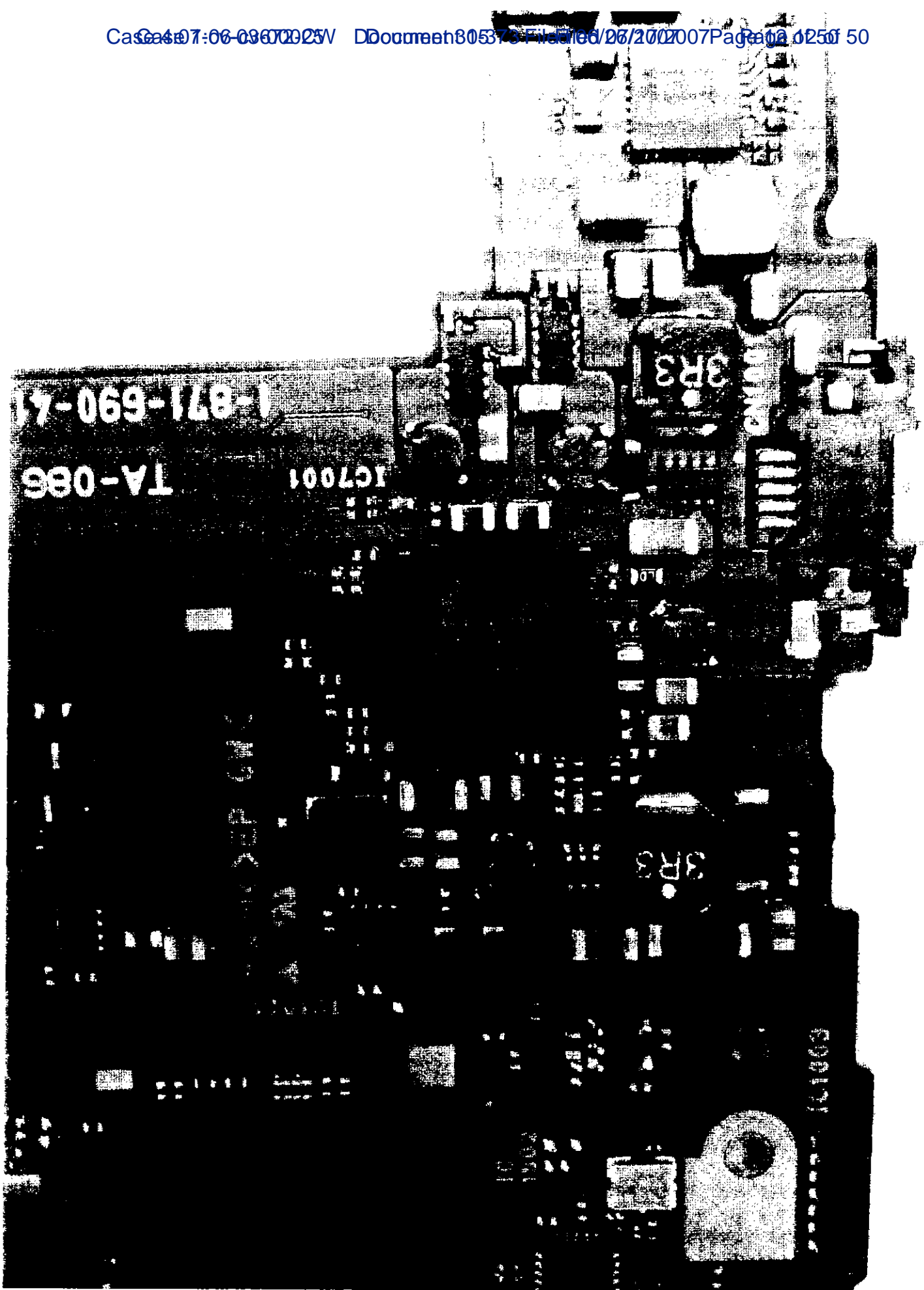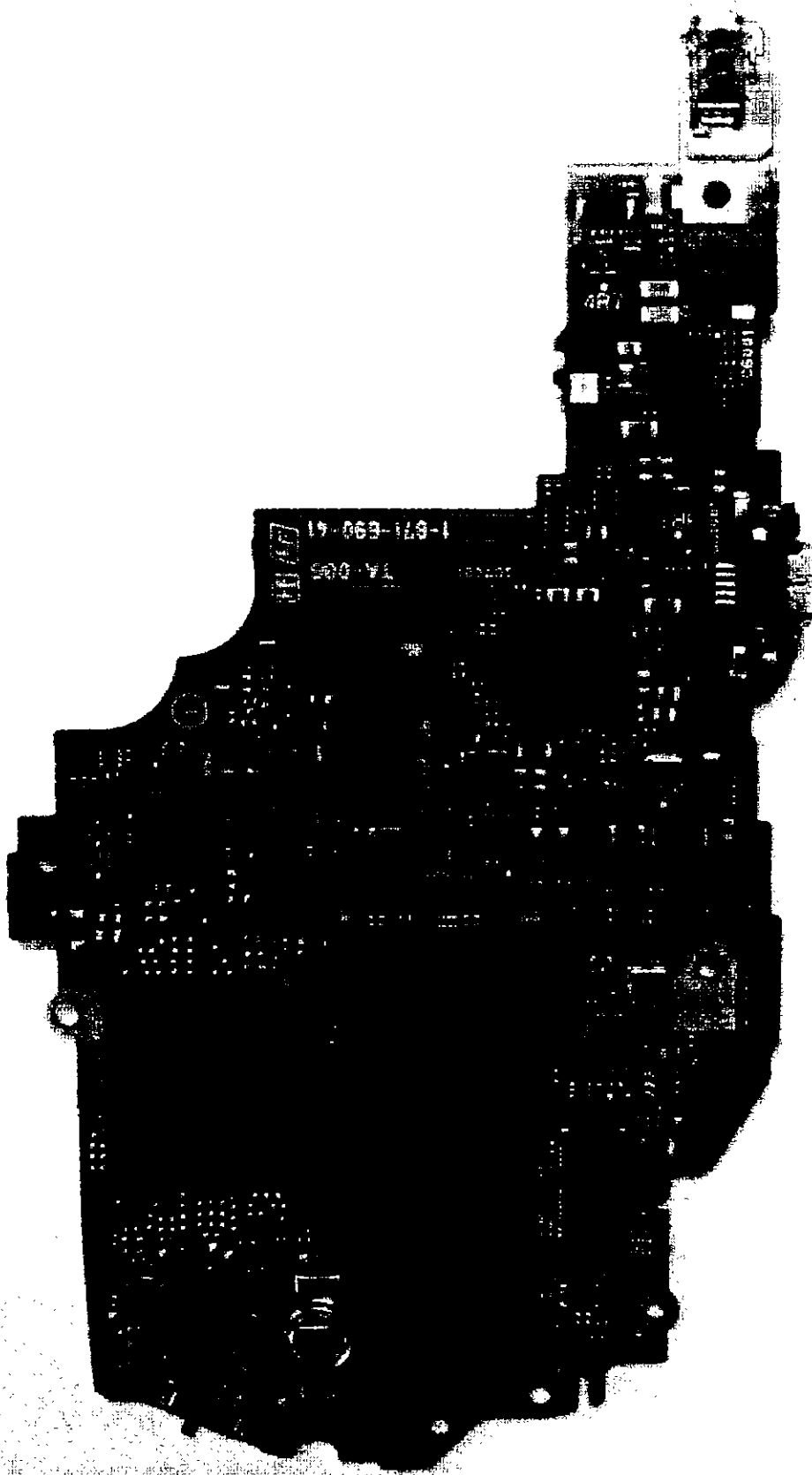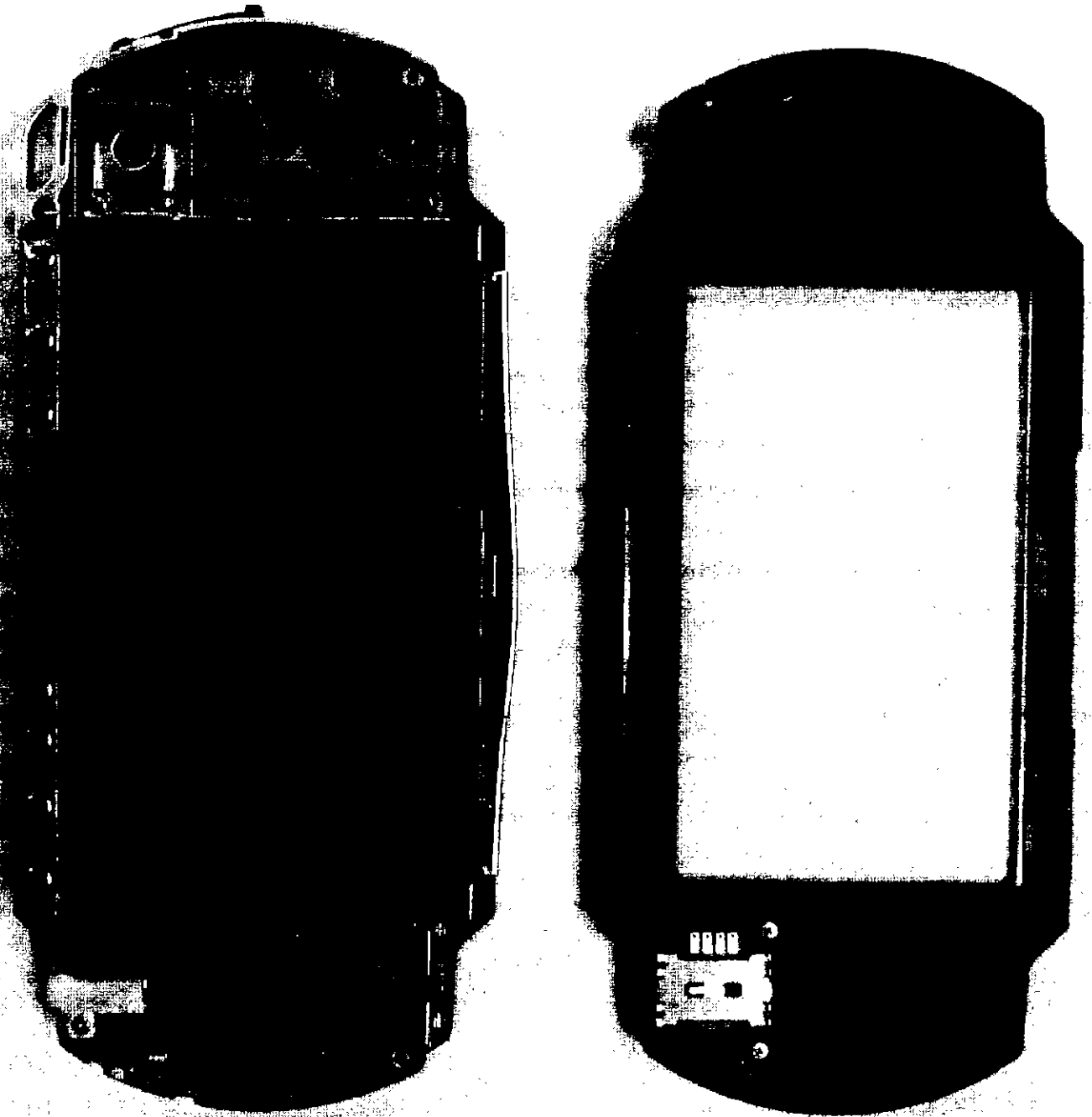
EXHIBIT C
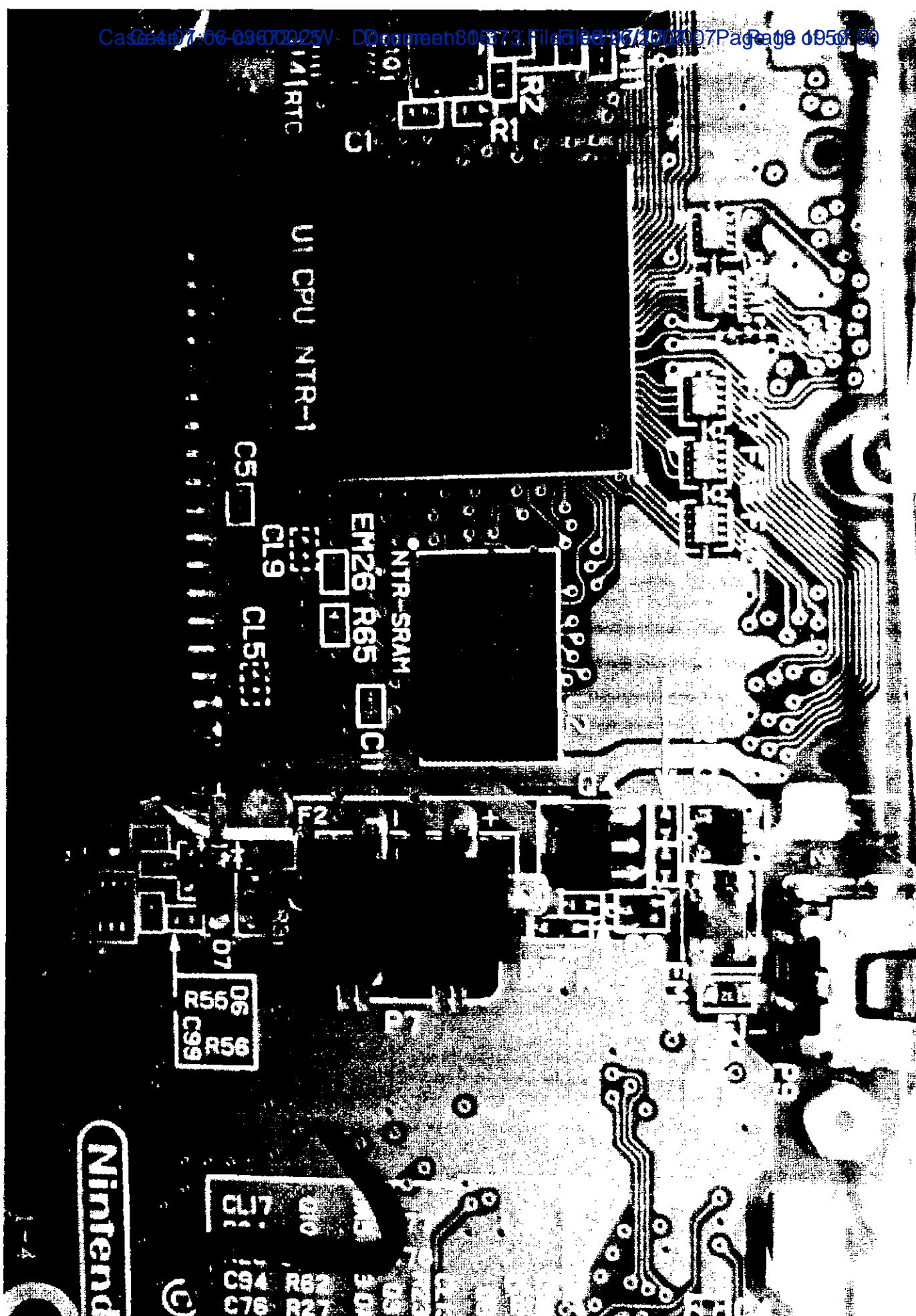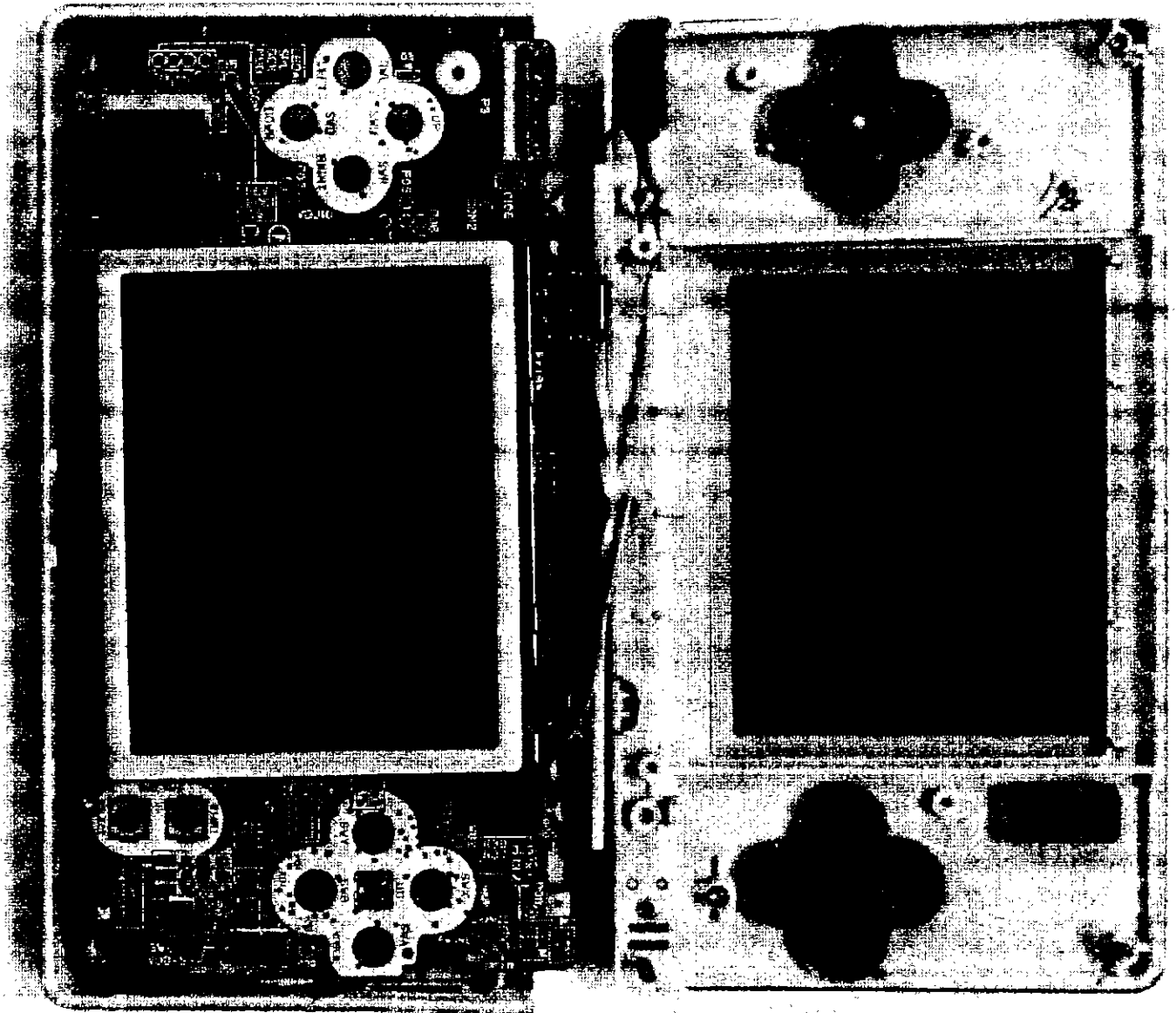
FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-11429-3E
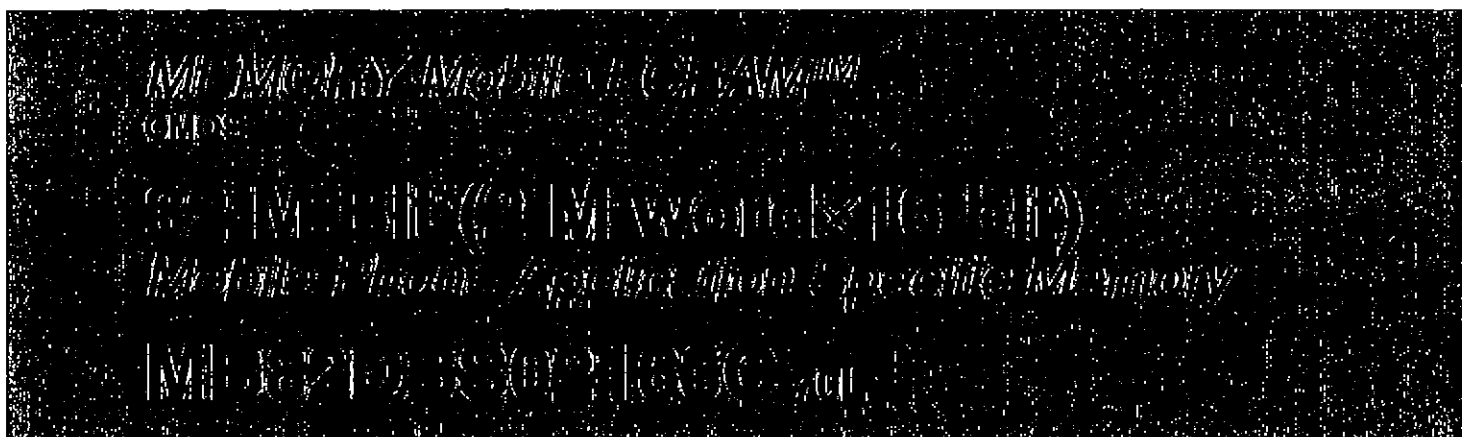
■ DESCRIPTION

The FUJITSU MB82DBS02163C is a CMOS Fast Cycle Random Access Memory (FCRAM*) with asynchronous Static Random Access Memory (SRAM) interface containing 33,554,432 storages accessible in a 16-bit format. MB82DBS02163C is utilized using a FUJITSU advanced FCRAM core technology and improved integration in comparison to regular SRAM. The MB82DBS02163C adopts asynchronous page mode and synchronous burst mode for fast memory access as user configurable options.

This MB82DBS02163C is suited for mobile applications such as Cellular Handset and PDA.

*: FCRAM is a trademark of Fujitsu Limited, Japan

■ FEATURES

- Asynchronous SRAM Interface
- Fast Access Time : t_{CE} = 70 ns Max
- 8 words Page Access Capability : t_{PAA} = 20 ns Max
- Burst Read/Write Access Capability : t_{AC} = 12 ns Max
- Low Voltage Operating Condition : V_{DD} = +1.65 V to +1.95 V
- Wide Operating Temperature : T_A = -30 °C to +85 °C
- Byte Control by $\overline{LB}$ and $\overline{UB}$
- Low-Power Consumption : I_{DDA1} = 30 mA Max
                          I_{DDS1} = 80 µA Max
- Various Power Down mode : Sleep
                            4 M-bit Partial
                            8 M-bit Partial
- Shipping Form : Wafer/Chip, 71-ball plastic FBGA package

FUJITSU

MB82DBS02163C-70L

■ PRODUCT LINEUP

Parameter	MB82DBS02163C-70L
Access Time (Max) (t_{CE}, t_{AA})	70 ns
CLK Access Time (Max) (t_{AC})	12 ns
Active Current (Max) (I_{DDA1})	30 mA
Standby Current (Max) (I_{DDS1})	80 µA
Power Down Current (Max) (I_{DDPS})	10 µA

■ PIN ASSIGNMENT

(TOP VIEW)

(BGA-71P-M03)

2
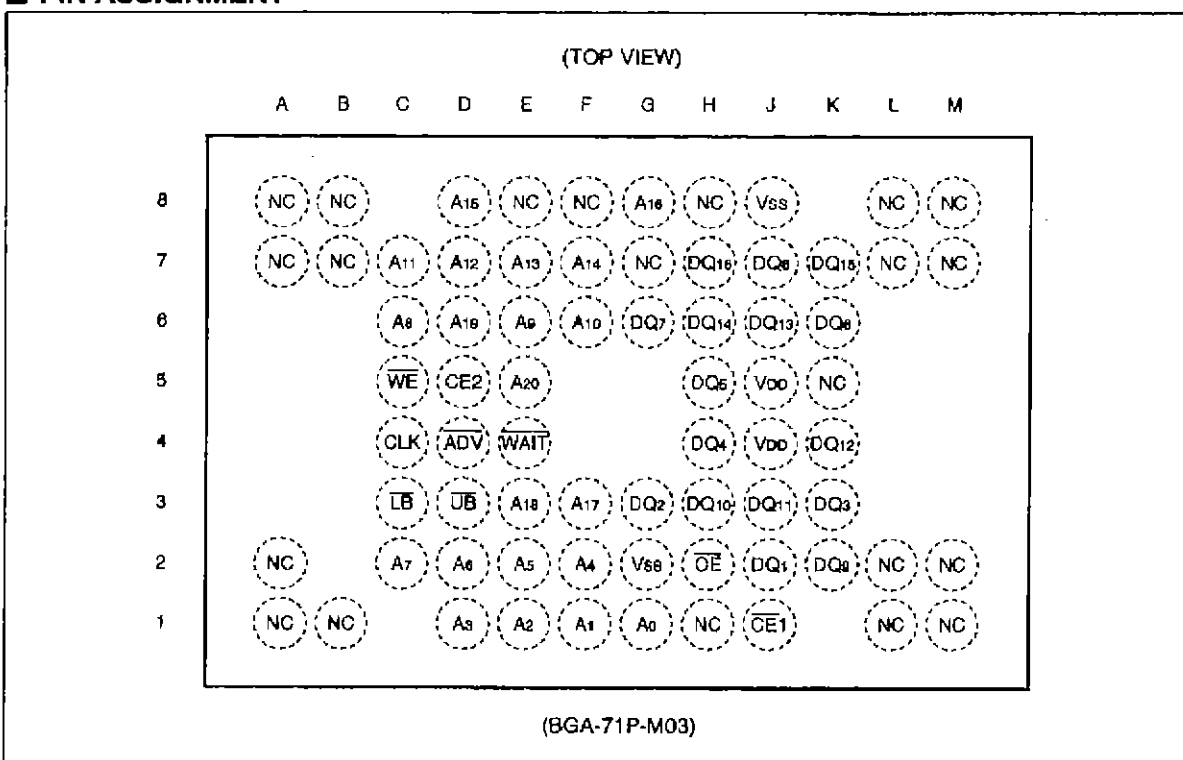
■ PIN DESCRIPTION

Pin Name	Description
A_{20} to A_0	Address Input
$\overline{CE1}$	Chip Enable 1 (Low Active)
CE2	Chip Enable 2 (High Active)
$\overline{WE}$	Write Enable (Low Active)
$\overline{OE}$	Output Enable (Low Active)
$\overline{LB}$	Lower Byte Control (Low Active)
$\overline{UB}$	Upper Byte Control (Low Active)
CLK	Clock Input
$\overline{ADV}$	Address Valid Input (Low Active)
$\overline{WAIT}$	Wait Output
DQ_8 to DQ_1	Lower Byte Data Input/Output
DQ_{16} to DQ_9	Upper Byte Data Input/Output
V_{DD}	Power Supply Voltage
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM

NTC0097688
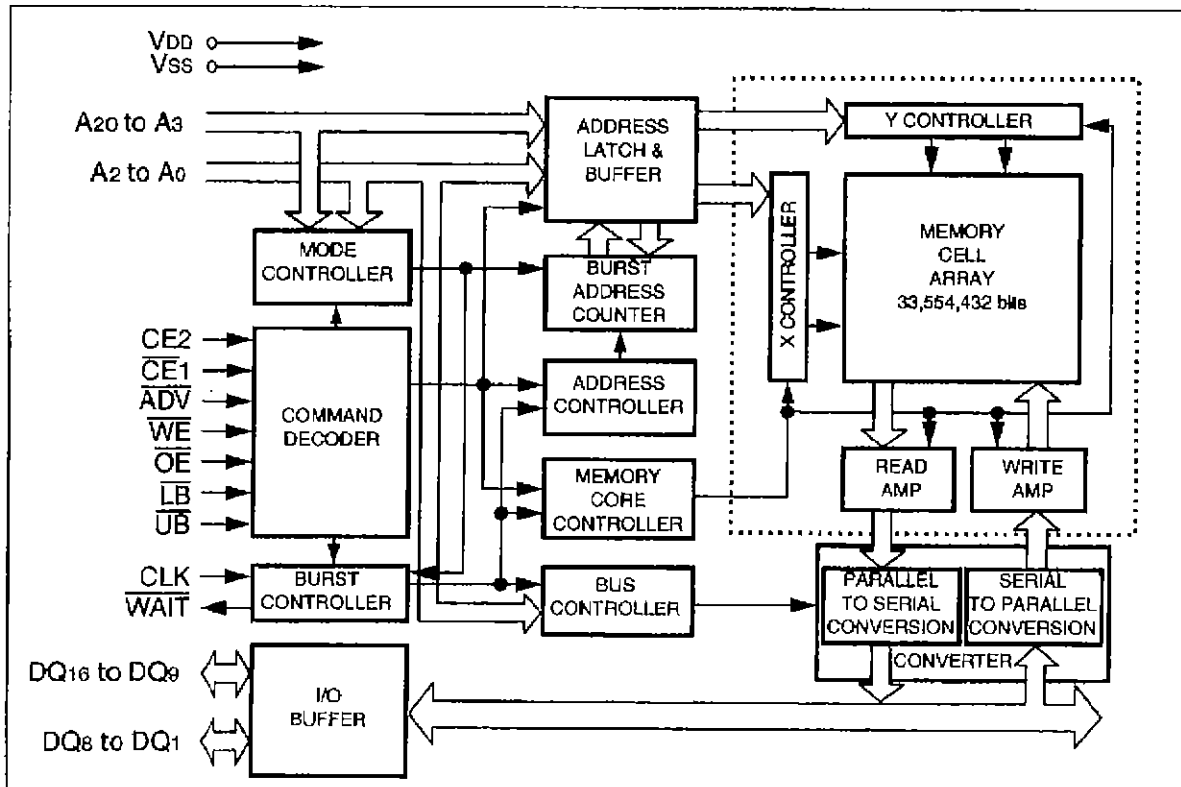
MB82DBS02163C-70L

■ FUNCTION TRUTH TABLE

1. Asynchronous Operation (Page Mode)

Mode	CE2	$\overline{CE1}$	CLK	$\overline{ADV}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	A_{20} to A_0	DQ_0 to DQ_1	DQ_{10} to DQ_9	$\overline{WAIT}$
Standby (Deselect)	H	H	X	X	X	X	X	X	X	High-Z	High-Z	High-Z
Output Disable*1	H	L	X	*3	H	H	X	X	*5	High-Z	High-Z	High-Z
Output Disable (No Read)			X	*3			H	H	Valid	High-Z	High-Z	High-Z
Read (Upper Byte)			X	*3			H	L	Valid	High-Z	Output Valid	High-Z
Read (Lower Byte)			X	*3	H	L	L	H	Valid	Output Valid	High-Z	High-Z
Read (Word)	H	L	X	*3			L	L	Valid	Output Valid	Output Valid	High-Z
Page Read			X	*3			L/H	L/H	Valid	*6	*6	High-Z
No Write			X	*3			H	H	Valid	Invalid	Invalid	High-Z
Write (Upper Byte)			X	*3			H	L	Valid	Invalid	Input Valid	High-Z
Write (Lower Byte)			X	*3	L	H*4	L	H	Valid	Input Valid	Invalid	High-Z
Write (Word)			X	*3			L	L	Valid	Input Valid	Input Valid	High-Z
Power Down*2	L	X	X	X	X	X	X	X	X	High-Z	High-Z	High-Z

Note : L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}, High-Z = High Impedance

*1: Should not be kept this logic condition longer than 1 μs.

*2: Power Down mode can be entered from Standby state and all output are in High-Z state.
Data retention depends on the selection of Partial Size for Power Down Program.
Refer to "Power Down" in "■FUNCTIONAL DESCRIPTION" for the details.

*3: "L" for address pass through and "H" for address latch on the rising edge of $\overline{ADV}$.

*4: $\overline{OE}$ can be V_{IL} during write operation if the following conditions are satisfied;
(1) Write pulse is initiated by $\overline{CE1}$. Refer to "(14) Asynchronous Read/Write Timing #1-1 ($\overline{CE1}$ Control)" in "■TIMING DIAGRAMS".
(2) $\overline{OE}$ stays V_{IL} during Write cycle.

*5: Can be either V_{IL} or V_{IH} but must be valid before Read or Write.

*6: Output of upper and lower byte data is either Valid or High-Z depending on the level of $\overline{LB}$ and $\overline{UB}$ input.

4

MB82DBS02163C-70L

2. Synchronous Operation (Burst Mode)

Mode	CE2	CE̅1̅	CLK	ADV	W̅E̅	O̅E̅	L̅B̅	U̅B̅	A20 to A0	DQ8 to DQ1	DQ16 to DQ9	W̅A̅I̅T̅
Standby(Deselect)		H	X	X	X	X	X	X	X	High-Z	High-Z	High-Z
Start Address Latch*1	H	L	↗*3	⌐	X*4	X*4			Valid*7	High-Z*8	High-Z*8	High-Z*11
Advance Burst Read to Next Address*1			↗*3		H	L				Output Valid*9	Output Valid*9	Output Valid
Burst Read Suspend*1			↗*3		H	H	X*6	X*6	X	High-Z	High-Z	High*12
Advance Burst Write to Next Address*1			↗*3	H	L*5	H				Input Valid*10	Input Valid*10	High*13
Burst Write Suspend*1			↗*3		H*5	H				Input Invalid	Input Invalid	High*12
Terminate Burst Read		↘	X		H	X				High-Z	High-Z	High-Z
Terminate Burst Write		↘	X		X	H				High-Z	High-Z	High-Z
Power Down*2	L	X	X	X	X	X	X	X	X	High-Z	High-Z	High-Z

Note : L = VIL, H = VIH, X can be either VIL or VIH, ↗ = valid edge, ⌐ = rising edge of Low pulse,
   High-Z = High impedance

*1: Should not be kept this logic condition longer than 8 μs.

*2: Power Down mode can be entered from Standby state and all output are in High-Z state.
   Data retention depends on the selection of Partial Size for Power Down Program.
   Refer to "Power Down" in "■FUNCTIONAL DESCRIPTION" for the details.

*3: Valid clock edge shall be set on either rising or falling edge through CR set. CLK must be started and stable prior to memory access.

*4: Can be either VIL or VIH except for the case the both of O̅E̅ and W̅E̅ are VIL.
   It is prohibited to bring the both of O̅E̅ and W̅E̅ to VIL.

*5: When device is operating in "W̅E̅ Single Clock Pulse Control" mode, W̅E̅ is Don't care once write operation is determined by W̅E̅ Low Pulse at the beginning of write access together with address latching. Burst write suspend feature is not supported in "W̅E̅ Single Clock Pulse Control" mode.

*6: Can be either VIL or VIH but must be valid before Read or Write is determined. And once L̅B̅ and U̅B̅ input levels are determined, they must not be changed until the end of burst.

*7: Once valid address is determined, input address must not be changed during A̅D̅V̅ = L.

*8: If O̅E̅ = L, output is either Invalid or High-Z depending on the level of L̅B̅ and U̅B̅ input. If W̅E̅ = L, input is Invalid.
   If O̅E̅ = W̅E̅ = H, output is High-Z.

*9: Outputs is either Valid or High-Z depending on the level of L̅B̅ and U̅B̅ input.

*10: Input is either Valid or Invalid depending on the level of L̅B̅ and U̅B̅ input.

*11: Output is either High-Z or Invalid depending on the level of O̅E̅ and W̅E̅ input.

*12: Keep the level from previous cycle except for suspending on last data. Refer to "W̅A̅I̅T̅ Output Function" in "■FUNCTIONAL DESCRIPTION" for the details.

*13: W̅A̅I̅T̅ output is driven in High level during burst write operation.

5

NTC0097690

MB82DBS02163C-70L

■ STATE DIAGRAM

• Initial/Standby State

Asynchronous Operation (Page Mode)

Synchronous Operation (Burst Mode)

Common State

Power Up → Pause Time

CR Set

@M = 1   @M = 0

Power Down   CE2 = H   Power Down

CE2 = L   Standby   CE2 = H   Standby   CE2 = L

• Asynchronous Operation

CE2 = $\overline{CE}$1 = H

Standby

$\overline{CE}$1 = L & $\overline{WE}$ = L $\overline{CE}$1 = L $\overline{CE}$1 = H $\overline{CE}$1 = L & $\overline{OE}$ = L

$\overline{CE}$1 = H   Output Disable $\overline{CE}$1 = H

Byte Control

$\overline{WE}$ = H $\overline{OE}$ = L

Write $\overline{WE}$ = L $\overline{OE}$ = H   Read

Byte Control @$\overline{OE}$ = L

Address Change or Byte Control

• Synchronous Operation

CE2 = $\overline{CE}$1 = H

Standby

$\overline{CE}$1 = H $\overline{CE}$1 = H

Write Suspend   Read Suspend

$\overline{CE}$1 = H $\overline{CE}$1 = H

$\overline{WE}$ = H $\overline{CE}$1 = L, $\overline{ADV}$ Low Pulse, & $\overline{WE}$ = L $\overline{CE}$1 = L, $\overline{ADV}$ Low Pulse, & $\overline{OE}$ = L $\overline{OE}$ = H

$\overline{WE}$ = L $\overline{OE}$ = L

$\overline{ADV}$ Low Pulse   Write   Read $\overline{ADV}$ Low Pulse

$\overline{ADV}$ Low Pulse (@BL = 8 or 16, and after burst operation is completed)

Note : Assuming all the parameters specified in AC CHARACTERISTICS are satisfied. Refer to the "■FUNCTIONAL DESCRIPTION", "2. AC Characteristics" in "■ELECTRICAL CHARACTERISTICS", and "■TIMING DIAGRAMS" for details.

6

MB82DBS02163C-70L

■ FUNCTIONAL DESCRIPTION

This device supports asynchronous read, page read & normal write operation and synchronous burst read and burst write operation for faster memory access and features 3 kinds of power down modes for power saving as user configurable option.

• Power-up

It is required to follow the power-up timing to start executing proper device operation. Refer to "Power-up Timing". After Power-up, the device defaults to asynchronous page read & normal write operation mode with sleep power down feature.

• Configuration Register

The Configuration Register(CR) is used to configure the type of device function among optional features. Each selection of features is set through CR set sequence after power-up. If CR set sequence is not performed after power-up, the device is configured for asynchronous operation with sleep power down feature as default configuration.

• CR Set Sequence

The CR set requires total 6 read/write cycles with unique address. Operation other than read/write operation requires that device being in standby mode. Following table shows the detail sequence.

Cycle #	Operation	Address	Data
#1	Read	1FFFFFh (MSB)	Read Data (RDa)
#2	Write	1FFFFFh	RDa
#3	Write	1FFFFFh	RDa
#4	Write	1FFFFFh	X
#5	Write	1FFFFFh	X
#6	Read	Address Key	Read Data (RDb)

The first cycle is to read from most significant address(MSB).

The second and third cycles are to write to MSB. If the second or third cycle is written into the different address, the CR set is cancelled and the data written by the second or third cycle is valid as a normal write operation. It is recommended to write back the data(RDa) read by first cycle to MSB in order to secure the data.

The forth and fifth cycles are to write to MSB. The data of forth and fifth cycle is don't-care. If the forth or fifth cycle is written into different address, the CR set is also cancelled, but write data may not be written as normal write operation.

The last cycle is to read from specific address key for mode selection. And read data(RDb) is invalid.

Once this CR set sequence is performed from an initial CR set to the other new CR set, the written data stored in memory cell array may be lost. So, it should perform the CR set sequence prior to regular read/write operation if necessary to change from default configuration.

7

NTC0097692

MB82DBS02163C-70L

• **Address Key**

The address key has the following format.

Address Pin	Register Name	Function	Key	Description	Note
A20, A19	PS	Partial Size	00	8 M-bit Partial	
			01	4 M-bit Partial	
			10	Reserved for future use	*1
			11	Sleep [Default]	
A18 to A10	BL	Burst Length	000	Reserved for future use	*1
			001	Reserved for future use	*1
			010	8 words	
			011	16 words	
			100	Reserved for future use	*1
			101	Reserved for future use	*1
			110	Reserved for future use	*1
			111	Continuous	
A15	M	Mode	0	Synchronous Mode (Burst Read / Write)	*2
			1	Asynchronous Mode [Default] (Page Read / Normal Write)	*3
A14 to A12	RL	Read Latency	000	Reserved for future use	*1
			001	3 clocks	
			010	4 clocks	
			011	5 clocks	
			1xx	Reserved for future use	*1
A11	BS	Burst Sequence	0	Reserved for future use	*1
			1	Sequential	
A10	SW	Single Write	0	Burst Read & Burst Write	
			1	Burst Read & Single Write	*4
A9	VE	Valid Clock Edge	0	Falling Clock Edge	
			1	Rising Clock Edge	
A8	—	—	1	Unused bits must be 1	*5
A7	WC	Write Control	0	$\overline{WE}$ Single Clock Pulse Control without Write Suspend Function	*4
			1	$\overline{WE}$ Level Control with Write Suspend Function	
A6 to A0	—	—	1	Unused bits must be 1	*5

*1: It is prohibited to apply this key.

*2: If M = 0, all the registers must be set with appropriate Key input at the same time.

*3: If M = 1, PS must be set with appropriate Key input at the same time. Except for PS, all the other key inputs must be "1".

*4: Burst Read & Single Write is not supported at $\overline{WE}$ Single Clock Pulse Control.

*5: A8 and A6 to A0 must be all "1" in any cases.

8

MB82DBS02163C-70L

• **Power Down**

The Power Down is low power idle state controlled by CE2. CE2 Low drives the device in power down mode and maintains low power idle state as long as CE2 is kept Low. CE2 High resumes the device from power down mode.

This device has 3 power down modes, Sleep, 4 M-bit Partial, and 8 M-bit Partial.

The selection of power down mode is set through CR set sequence. Each mode has following data retention features.

Mode	Data Retention Size	Retention Address
Sleep [default]	No	N/A
4 M-bit Partial	4 M bits	000000h to 03FFFFh
8 M-bit Partial	8 M bits	000000h to 07FFFFh

The default state after power-up is Sleep and it is the lowest power consumption but all data will be lost once CE2 is brought to Low for Power Down. It is not required to perform CR set sequence to set to Sleep mode after power-up in case of asynchronous operation.

• **Burst Read/Write Operation**

Synchronous burst read/write operation provides faster memory access that synchronized to microcontroller or system bus frequency. Configuration Register(CR) Set is required to perform burst read & write operation after power-up. Once CR set sequence is performed to select synchronous burst mode, the device is configured to synchronous burst read/write operation mode with corresponding RL and BL that is set through CR set sequence together with operation mode. In order to perform synchronous burst read & write operation, it is required to control new signals, CLK, $\overline{ADV}$ and $\overline{WAIT}$ that Low Power SRAMs do not have.

• Burst Read Operation

(Continued)

9

NTC0097694
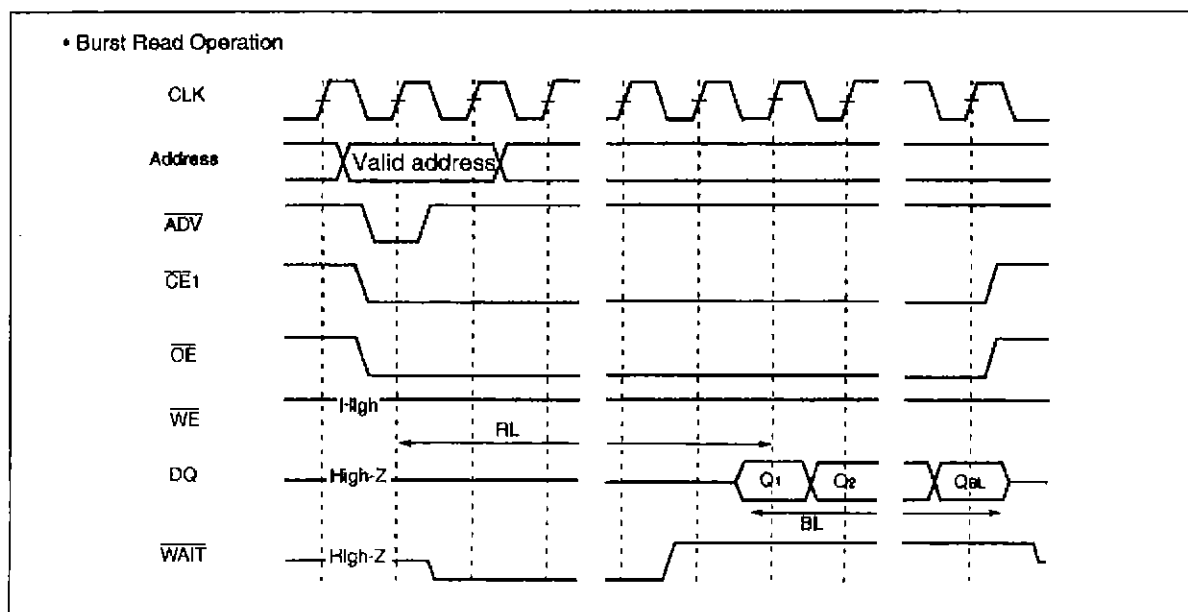
MB82DBS02163C-70L

(Continued)

- Burst Write Operation
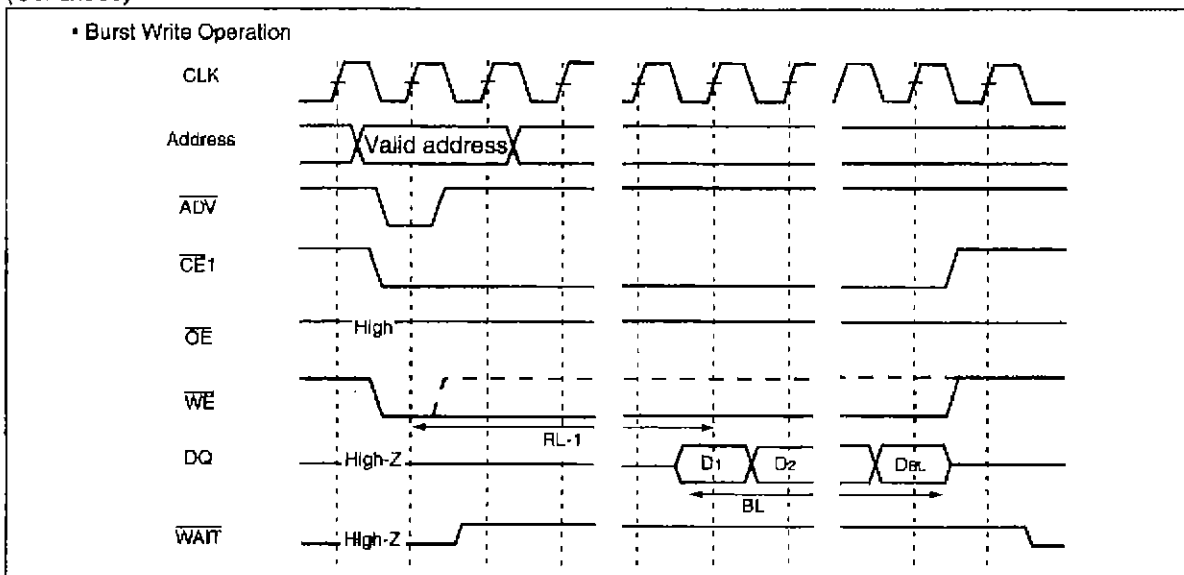
• CLK Input Function

The CLK is input signal to synchronize memory to microcontroller or system bus frequency during synchronous burst read & write operation. The CLK input increments device internal address counter and the valid edge of CLK is referred for latency counts from address latch, burst write data latch, and burst read data output. During synchronous operation mode, CLK input must be supplied except for standby state and power down state. CLK is Don't care during asynchronous operation.

• $\overline{ADV}$ Input Function

The $\overline{ADV}$ is input signal to latch valid address. It is applicable to synchronous operation as well as asynchronous operation. $\overline{ADV}$ input is active during $\overline{CE1}$ = L and $\overline{CE1}$ = H disables $\overline{ADV}$ input. All addresses are determined on the rising edge of $\overline{ADV}$.

During synchronous burst read/write operation, $\overline{ADV}$ = H disables all address inputs. Once $\overline{ADV}$ is brought to High after valid address latch, it is inhibited to bring $\overline{ADV}$ Low until the end of burst or until burst operation is terminated. $\overline{ADV}$ Low pulse is mandatory for synchronous burst read/write operation mode to latch the valid address input.

During asynchronous operation, $\overline{ADV}$ = H also disables all address inputs. $\overline{ADV}$ can be tied to Low during asynchronous operation and it is not necessary to control $\overline{ADV}$ to High.

10

- **WAIT Output Function**

The $\overline{\text{WAIT}}$ is output signal to indicate data bus status when the device is operating in synchronous burst mode.

During burst read operation, $\overline{\text{WAIT}}$ output is enabled after specified time duration from $\overline{\text{OE}}$ = L or $\overline{\text{CE1}}$ = L whichever occurs last. $\overline{\text{WAIT}}$ output Low indicates data output at next clock cycle is invalid, and $\overline{\text{WAIT}}$ output becomes High one clock cycle prior to valid data output. During continuous burst read operation, an additional output delay may occur when a burst sequence crosses it's device-row boundary. The $\overline{\text{WAIT}}$ output notifies this delay to controller. Refer to the section "Burst Length" for the additional delay cycles in details. During $\overline{\text{OE}}$ read suspend, $\overline{\text{WAIT}}$ output does not indicate data bus status but carries the same level from previous clock cycle (kept High) except for read suspend on the final data output. If final read data output is suspended, $\overline{\text{WAIT}}$ output becomes high impedance after specified time duration from $\overline{\text{OE}}$ = H.

During burst write operation, $\overline{\text{WAIT}}$ output is enabled to High level after specified time duration from $\overline{\text{WE}}$ = L or $\overline{\text{CE1}}$ = L whichever occurs last and kept High for entire write cycles including $\overline{\text{WE}}$ write suspend. The actual write data latching starts on the appropriate clock edge with respect to Valid Clock Edge, Read Latency, and Burst Length. During $\overline{\text{WE}}$ Write suspend, $\overline{\text{WAIT}}$ output does not indicate data bus status but carries the same level from previous clock cycle (kept High) except for write suspend on the final data input. If final write data input is suspended, $\overline{\text{WAIT}}$ output becomes high impedance after specified time duration from $\overline{\text{WE}}$ = H.

The burst operation is always started after fixed latency with respect to Read Latency set in CR.

When the device is operating in asynchronous mode, $\overline{\text{WAIT}}$ output is always in High Impedance.

11

MB82DBS02163C-70L

- **Latency**

    Read Latency (RL) is the number of clock cycles between the address being latched and first read data becoming available during synchronous burst read operation. It is set through CR set sequence after power-up. Once specific RL is set through CR set sequence, write latency, that is the number of clock cycles between address being latched and first write data being latched, is automatically set to RL-1. The burst operation is always started after fixed latency with respect to Read Latency set in CR.
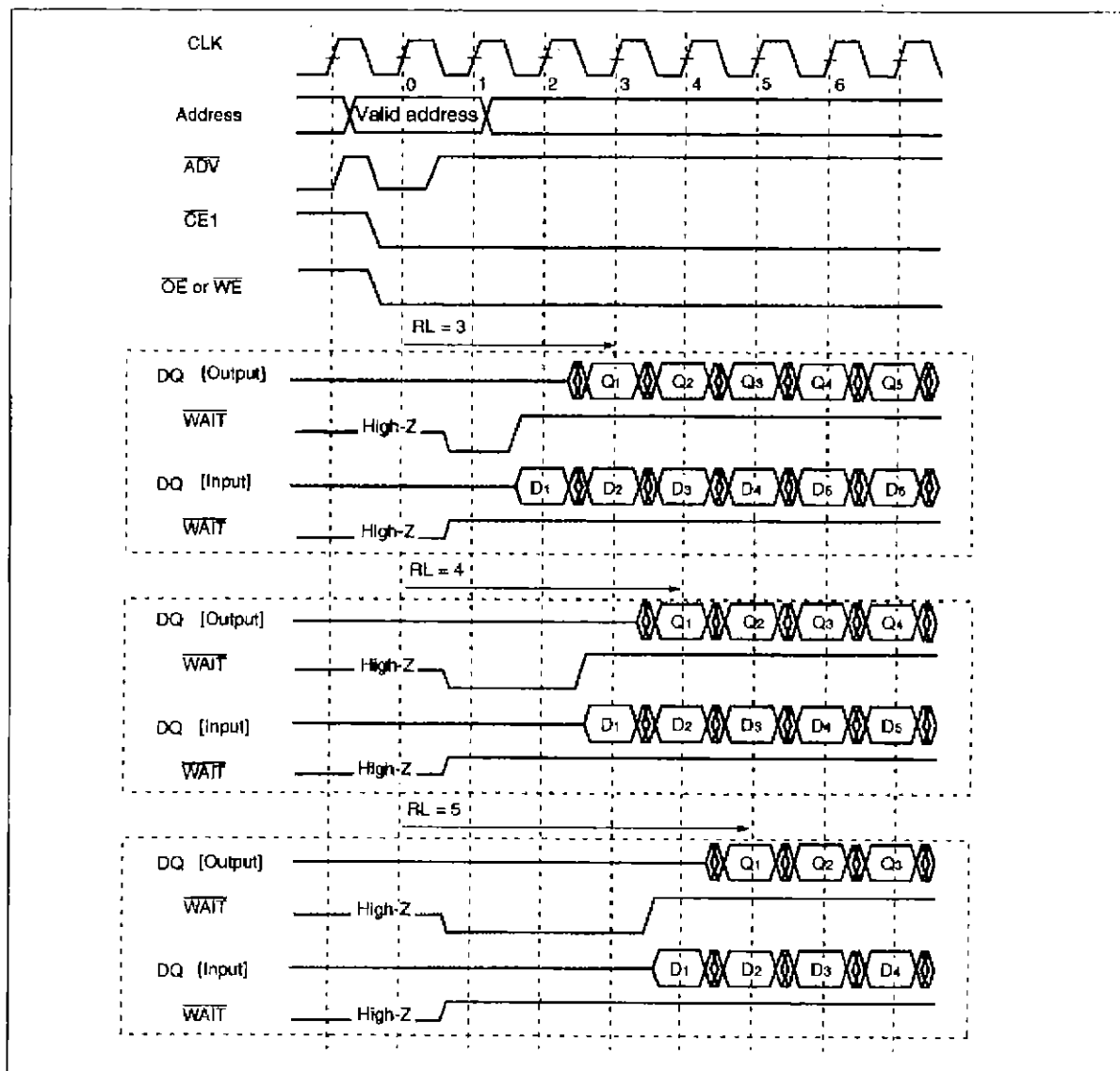
• Address Latch by ADV̅

The ADV̅ latches valid address presence on address inputs. During synchronous burst read/write operation mode, all the address are determined on the rising edge of ADV̅ when CE̅1 = L. The specified minimum value of ADV̅ = L setup time and hold time against valid edge of clock where RL count is begun must be satisfied. Valid address must be determined with specified setup time against either the falling edge of ADV̅ or falling edge of CE̅1 whichever comes late. And the determined valid address must not be changed during ADV̅ = L period.

• Burst Length

Burst Length is the number of word to be read or written during synchronous burst read/write operation as the result of a single address latch cycle. It can be set on 8,16 words boundary or continuous for entire address through CR set sequence. The burst type is sequential that is incremental decoding scheme within a boundary address. Starting from initial address being latched, device internal address counter assigns +1 to the previous address until reaching the end of boundary address and then wrap round to least significant address (= 0). After completing read data output or write data latch for the set burst length, operation automatically ended except for continuous burst length. When continuous burst length is set, read/write is endless unless it is terminated by the rising edge of CE̅1. During continuous burst read, an additional output delay may occur when a burst sequence cross it's device-row boundary. This is the case when A0 to A8 of starting address is either 7Dh, 7Eh, or 7Fh as shown in the following table. The WAIT̅ signal indicates this delay.

Start Address	Read Address Sequence		
(A8 to A0)	BL = 8	BL = 16	Continuous
00h	00-01-02-...-06-07	00-01-02-...-0E-0F	00-01-02-03-04-...
01h	01-02-03-...-07-00	01-02-03-...-0F-00	01-02-03-04-05-...
02h	02-03-...-07-00-01	02-03-...-0F-00-01	02-03-04-05-06-...
03h	03-...-07-00-01-02	03-...-0F-00-01-02	03-04-05-06-07-...
...	...	...	...
7Ch	7C-...-7F-78-...-7B	7C-...-7F-70-...-7B	7C-7D-7E-7F-80-81-...
7Dh	7D-7E-7F-78-...-7C	7D-7E-7F-70-...-7C	7D-7E-7F-WAIT-80-81-...
7Eh	7E-7F-78-79-...-7D	7E-7F-70-71-...-7D	7E-7F-WAIT-WAIT-80-81-...
7Fh	7F-78-79-7A-...-7E	7F-70-71-72-...-7E	7F-WAIT-WAIT-WAIT-80-81

Note : Read address In Hexadecimal

• Single Write

Single write is synchronous write operation with Burst Length = 1. The device can be configured either to "Burst Read & Single Write" or to "Burst Read & Burst Write" through CR set sequence. Once the device is configured to "Burst Read & Single Write" mode, the burst length for synchronous write operation is always fixed 1 regardless of BL values set in CR, while burst length for read Is in accordance with BL values set in CR.

13

MB82DBS02163C-70L

• **Write control**

The device has two types of $\overline{WE}$ signal control method, "$\overline{WE}$ Level Control" and "$\overline{WE}$ Single Clock Pulse Control", for synchronous burst write operation. It is configured through CR set sequence.

● **Burst Read Suspend**

Burst read operation can be suspended by $\overline{OE}$ High pulse. During burst read operation, $\overline{OE}$ brought to High from Low suspends burst read operation. Once $\overline{OE}$ is brought to High with the specified setup time against clock where the data being suspended, the device internal counter is suspended, and the data output becomes high impedance after specified time duration. It is inhibited to suspend the first data output at the beginning of burst read.

$\overline{OE}$ brought to Low from High resumes burst read operation. Once $\overline{OE}$ is brought to Low, data output becomes valid after specified time duration, and internal address counter is reactivated. The last data output being suspended as the result of $\overline{OE}$ = H and first data output as the result of $\overline{OE}$ = L are from the same address.

In order to guarantee to output last data before suspension and first data after resumption, the specified minimum value of $\overline{OE}$ hold time and setup time against clock edge must be satisfied respectively.

● **Burst Write Suspend**

Burst write operation can be suspended by $\overline{WE}$ High pulse. During burst write operation, $\overline{WE}$ brought to High from Low suspends burst write operation. Once $\overline{WE}$ is brought to High with the specified setup time against clock where the data being suspended, device internal counter is suspended, data input is ignored. It is inhibited to suspend the first data input at the beginning of burst write.

$\overline{WE}$ brought to Low from High resumes burst write operation. Once $\overline{WE}$ is brought to Low, data input becomes valid after specified time duration, and internal address counter is reactivated. The write address of the cycle where data being suspended and the first write address as the result of $\overline{WE}$ = L are the same address.

In order to guarantee to latch the last data input before suspension and first data input after resumption, the specified minimum value of $\overline{WE}$ hold time and setup time against clock edge must be satisfied respectively.

Burst write suspend function is available when the device is operating in $\overline{WE}$ level controlled burst write only.

15

NTC0097700

MB82DBS02163C-70L

• **Burst Read Termination**

Burst read operation can be terminated by $\overline{CE}1$ brought to High. If BL is set on Continuous, burst read operation is continued endless unless terminated by $\overline{CE}1$ = H. It is inhibited to terminate burst read before first data output is completed. In order to guarantee last data output, the specified minimum value of $\overline{CE}1$ = L hold time from clock edge must be satisfied. After termination, the specified minimum recovery time is required to start new access.

• **Burst Write Termination**
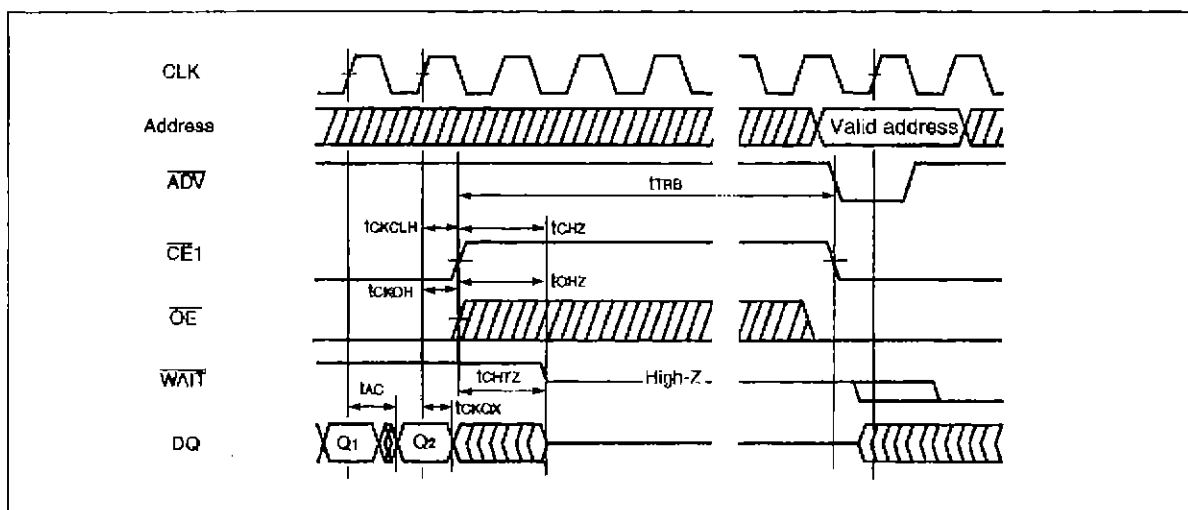
Burst write operation can be terminated by $\overline{CE}1$ brought to High. If BL is set on Continuous, burst write operation is continued endless unless terminated by $\overline{CE}1$ = H. It is inhibited to terminate burst write before first data input is completed. In order to guarantee last data input being latched, the specified minimum values of $\overline{CE}1$ = L hold time from clock edge must be satisfied. After termination, the specified minimum recovery time is required to start new access.

16

NTC0097701
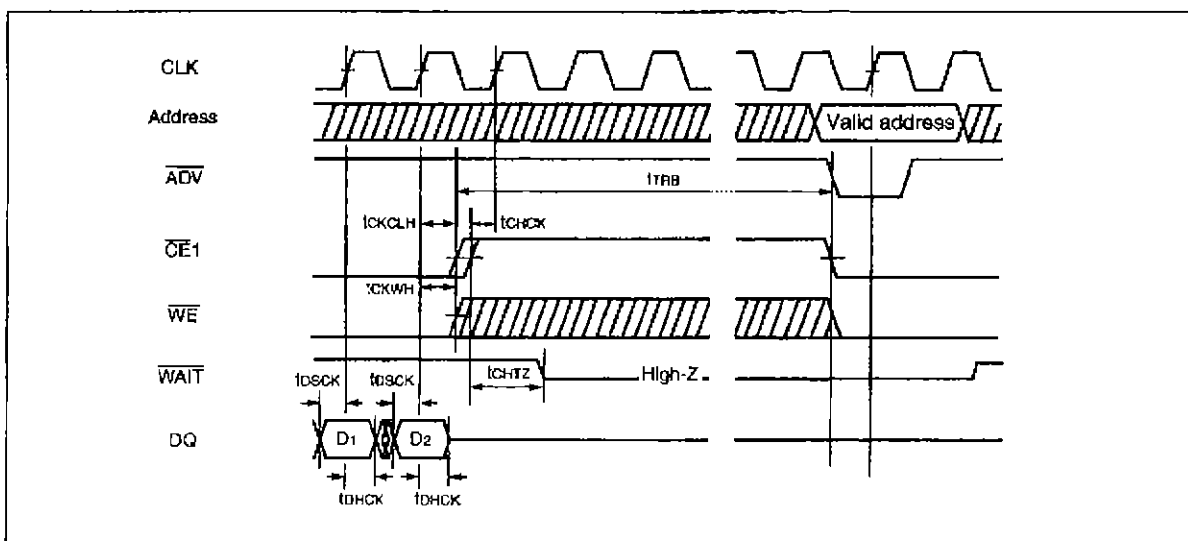
MB82DBS02163C-70L

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Voltage of V_{DD} Supply Relative to V_{SS}*	V_{DD}	− 0.5	+ 3.6	V
Voltage at Any Pin Relative to V_{SS}*	V_{IN}, V_{OUT}	− 0.5	+ 3.6	V
Short Circuit Output Current *	I_{OUT}	− 50	+ 50	mA
Storage Temperature	T_{STG}	− 55	+ 125	°C

* : All voltages are referenced to V_{SS} = 0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value		Unit
		Min	Max	
Power Supply Voltage*1	V_{DD}	1.65	1.95	V
	V_{SS}	0	0	V
High Level Input Voltage*1, *2	V_{IH}	$V_{DD} \times 0.8$	$V_{DD} + 0.2$	V
Low Level Input Voltage*1, *3	V_{IL}	− 0.3	$V_{DD} \times 0.2$	V
Ambient Temperature	T_A	− 30	+ 85	°C

*1 : All voltages are referenced to V_{SS} = 0 V.

*2 : Maximum DC voltage on input and I/O pins is V_{DD} + 0.2 V. During voltage transitions, inputs may overshoot to V_{DD} + 1.0 V for the periods of up to 5 ns.

*3 : Minimum DC voltage on input or I/O pins is -0.3 V. During voltage transitions, inputs may undershoot V_{SS} to -1.0 V for the periods of up to 5 ns.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ PACKAGE CAPACITANCE

(f = 1 MHz, T_A = +25 °C)

Parameter	Symbol	Test conditions	Value			Unit
			Min	Typ	Max	
Address Input Capacitance	C_{IN1}	V_{IN} = 0 V	—	—	5	pF
Control Input Capacitance	C_{IN2}	V_{IN} = 0 V	—	—	5	pF
Data Input/Output Capacitance	$C_{I/O}$	V_{IO} = 0 V	—	—	8	pF

17

MB82DBS02163C-70L

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(At recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions		Value Min	Value Max	Unit
Input Leakage Current	I_{LI}	$V_{SS} \leq V_{IN} \leq V_{DD}$		−1.0	+1.0	μA
Output Leakage Current	I_{LO}	$0\,V \leq V_{OUT} \leq V_{DD}$, Output Disable		−1.0	+1.0	μA
Output High Voltage Level	V_{OH}	$V_{DD} = V_{DD}$ (Min), $I_{OH} = -0.5\,mA$		1.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 1\,mA$		—	0.4	V
V_{DD} Power Down Current	I_{DDP8}	$V_{DD} = V_{DD}$ (Max), $V_{IN} = V_{IH}$ or V_{IL}, $CE2 \leq 0.2\,V$	SLEEP	—	10	μA
	I_{DDP4}		4 M-bit Partial	—	40	μA
	I_{DDP8}		8 M-bit Partial	—	50	μA
V_{DD} Standby Current	I_{DDS}	$V_{DD} = V_{DD}$ (Max), V_{IN} (including CLK) = V_{IH} or V_{IL}, $\overline{CE1} = CE2 = V_{IH}$		—	1.5	mA
	I_{DDS1}	$V_{DD} = V_{DD}$ (Max), V_{IN} (including CLK) $\leq 0.2\,V$ or V_{IN} (including CLK) $\geq V_{DD} - 0.2\,V$, $\overline{CE1} = CE2 \geq V_{DD} - 0.2\,V$		—	80	μA
	I_{DDS2}	$V_{DD} = V_{DD}$ (Max), t_{CK} = Min $V_{IN} \leq 0.2\,V$ or $V_{IN} \geq V_{DD} - 0.2\,V$, $\overline{CE1} = CE2 \geq V_{DD} - 0.2\,V$		—	200	μA
V_{DD} Active Current	I_{DDA1}	$V_{DD} = V_{DD}$ (Max), $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE1} = V_{IL}$ and $CE2 = V_{IH}$, $I_{OUT} = 0\,mA$	t_{RC}/t_{WC} = Min	—	30	mA
	I_{DDA2}		$t_{RC}/t_{WC} = 1\,μs$	—	3	mA
V_{DD} Page Read Current	I_{DDA3}	$V_{DD} = V_{DD}$ (Max), $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE1} = V_{IL}$ and $CE2 = V_{IH}$, $I_{OUT} = 0\,mA$, t_{PRC} = Min		—	10	mA
V_{DD} Burst Access Current	I_{DDA4}	$V_{DD} = V_{DD}$ (Max), $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE1} = V_{IL}$ and $CE2 = V_{IH}$, $t_{CK} = t_{CK}$ (Min), BL = Continuous, $I_{OUT} = 0\,mA$		—	15	mA

Notes : • All voltages are referenced to $V_{SS} = 0\,V$.
• I_{DD} depends on the output termination, load conditions, and AC characteristics.
• After power on, initialization following POWER-UP timing is required. DC characteristics are guaranteed after the initialization.

18

2. AC Characteristics

(1) Asynchronous Read Operation (Page mode)

(At recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
Read Cycle Time	t_{RC}	70	1000	ns	*1, *2
$\overline{CE}$1 Access Time	t_{CE}	—	70	ns	*3
$\overline{OE}$ Access Time	t_{OE}	—	40	ns	*3
Address Access Time	t_{AA}	—	70	ns	*3, *5
$\overline{ADV}$ Access Time	t_{AV}	—	70	ns	*3
$\overline{LB}$, $\overline{UB}$ Access Time	t_{BA}	—	30	ns	*3
Page Address Access Time	t_{PAA}	—	20	ns	*3, *6
Page Read Cycle Time	t_{PRC}	20	1000	ns	*1, *6, *7
Output Data Hold Time	t_{OH}	5	—	ns	*3
$\overline{CE}$1 Low to Output Low-Z	t_{CLZ}	5	—	ns	*4
$\overline{OE}$ Low to Output Low-Z	t_{OLZ}	10	—	ns	*4
$\overline{LB}$, $\overline{UB}$ Low to Output Low-Z	t_{BLZ}	0	—	ns	*4
$\overline{CE}$1 High to Output High-Z	t_{CHZ}	—	14	ns	*3
$\overline{OE}$ High to Output High-Z	t_{OHZ}	—	14	ns	*3
$\overline{LB}$, $\overline{UB}$ High to Output High-Z	t_{BHZ}	—	14	ns	*3
Address Setup Time to $\overline{CE}$1 Low	t_{ASC}	−5	—	ns	
Address Setup Time to $\overline{OE}$ Low	t_{ASO}	10	—	ns	
$\overline{ADV}$ Low Pulse Width	t_{VPL}	10	—	ns	*8
$\overline{ADV}$ High Pulse Width	t_{VPH}	15	—	ns	*8
Address Setup Time to $\overline{ADV}$ High	t_{ABV}	5	—	ns	
Address Hold Time from $\overline{ADV}$ High	t_{AHV}	10	—	ns	
Address Invalid Time	t_{IX}	—	10	ns	*5, *9
Address Hold Time from $\overline{CE}$1 High	t_{CHAH}	−5	—	ns	*10
Address Hold Time from $\overline{OE}$ High	t_{OHAH}	−5	—	ns	
$\overline{WE}$ High to $\overline{OE}$ Low Time for Read	t_{WHOL}	15	1000	ns	*11
$\overline{CE}$1 High Pulse Width	t_{CP}	15	—	ns	

*1 : Maximum value is applicable if $\overline{CE}$1 is kept at Low without change of address input of A_{20} to A_3.

*2 : Address should not be changed within minimum t_{RC}.

*3 : The output load 50 pF with 50 Ω termination to V_{DD} × 0.5 V.

*4 : The output load 5 pF without any other load.

*5 : Applicable to A_{20} to A_3 when $\overline{CE}$1 is kept at Low.

*6 : Applicable only to A_2, A_1 and A_0 when $\overline{CE}$1 is kept at Low for the page address access.

(Continued)

19

MB82DBS02163C-70L

(Continued)

*7 : In case Page Read Cycle is continued with keeping $\overline{CE}1$ stays Low, $\overline{CE}1$ must be brought to High within 4 μs. In other words, Page Read Cycle must be closed within 4 μs.

*8 : t_{VPL} is specified from the falling edge of either $\overline{CE}1$ or $\overline{ADV}$ whichever comes late. The sum of t_{VPL} and t_{VPH} must be equal or greater than t_{RC} for each access.

*9 : Applicable to address access when at least two of address inputs are switched from previous state.

*10 : t_{RC} (Min) and t_{PAC} (Min) must be satisfied.

*11 : If actual value of t_{WHOL} is shorter than specified minimum values, the actual t_{AA} of following Read may become longer by the amount of subtracting actual value from specified minimum value.

20

(2) Asynchronous Write Operation

(At recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
Write Cycle Time	t_{WC}	70	1000	ns	*1, *2
Address Setup Time	t_{AS}	0	—	ns	*3
$\overline{ADV}$ Low Pulse Width	t_{VPL}	10	—	ns	*4
$\overline{ADV}$ High Pulse Width	t_{VPH}	15	—	ns	*4
Address Setup Time to $\overline{ADV}$ High	t_{ASV}	5	—	ns	
Address Hold Time from $\overline{ADV}$ High	t_{AHV}	10	—	ns	
$\overline{CE}1$ Write Pulse Width	t_{CW}	45	—	ns	*3
$\overline{WE}$ Write Pulse Width	t_{WP}	45	—	ns	*3
$\overline{LB}, \overline{UB}$ Write Pulse Width	t_{BW}	45	—	ns	*3
$\overline{LB}, \overline{UB}$ Byte Mask Setup Time	t_{BS}	–5	—	ns	*5
$\overline{LB}, \overline{UB}$ Byte Mask Hold Time	t_{BH}	–5	—	ns	*6
Write Recovery Time	t_{WR}	0	—	ns	*7
$\overline{CE}1$ High Pulse Width	t_{CP}	15	—	ns	
$\overline{WE}$ High Pulse Width	t_{WHP}	15	1000	ns	
$\overline{LB}, \overline{UB}$ High Pulse Width	t_{BHP}	15	1000	ns	
Data Setup Time	t_{DS}	15	—	ns	
Data Hold Time	t_{DH}	0	—	ns	
$\overline{OE}$ High to $\overline{CE}1$ Low Setup Time for Write	t_{OHCL}	–5	—	ns	*8
$\overline{OE}$ High to Address Setup Time for Write	t_{OEB}	0	—	ns	*9
$\overline{LB}$ and $\overline{UB}$ Write Pulse Overlap	t_{BWO}	30	—	ns	

*1 : Maximum value is applicable if $\overline{CE}1$ is kept at Low without any address change.

*2 : Minimum value must be equal or greater than the sum of write pulse width (t_{CW}, t_{WP} or t_{BW}) and write recovery time (t_{WR}).

*3 : Write pulse width is defined from High to Low transition of $\overline{CE}1$, $\overline{WE}$, $\overline{LB}$, or $\overline{UB}$, whichever occurs last.

*4 : t_{VPL} is specified from the falling edge of either $\overline{CE}1$ or $\overline{ADV}$ whichever comes late. The sum of t_{VPL} and t_{VPH} must be equal or greater than t_{WC} for each access.

*5: Applicable for byte mask only. Byte mask setup time is defined from the High to Low transition of $\overline{CE}1$ or $\overline{WE}$ whichever occurs last.

*6: Applicable for byte mask only. Byte mask hold time is defined from the Low to High transition of $\overline{CE}1$ or $\overline{WE}$ whichever occurs first.

*7: Write recovery time is defined from Low to High transition of $\overline{CE}1$, $\overline{WE}$, $\overline{LB}$, or $\overline{UB}$, whichever occurs first.

*8: If $\overline{OE}$ is Low after minimum t_{OHCL}, read cycle is initiated. In other word, $\overline{OE}$ must be brought to High within 5 ns after $\overline{CE}1$ is brought to Low.

*9: If $\overline{OE}$ is Low after new address input, read cycle is initiated. In other word, $\overline{OE}$ must be brought to High at the same time or before new address is valid.

21

NTC0097706

MB82DBS02163C-70L

(3) Synchronous Operation - Clock Input (Burst mode)

(At recommended operating conditions unless otherwise noted)

Parameter		Symbol	Value		Unit	Notes
			Min	Max		
Clock Period	RL = 5	t_{CK}	15	—	ns	*1
	RL = 4		20	—	ns	*1
	RL = 3		30	—	ns	*1
Clock High Pulse Width		t_{CKH}	5	—	ns	
Clock Low Pulse Width		t_{CKL}	5	—	ns	
Clock Transition Time		t_{CKT}	—	3	ns	*2

*1: Clock period is defined between valid clock edges.

*2: Clock transition time is defined between V_{IH} (Min) and V_{IL} (Max)

(4) Synchronous Operation - Address Latch (Burst mode)

(At recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
Address Setup Time to $\overline{CE1}$ Low	t_{ASCL}	−5	—	ns	*1
Address Setup Time to $\overline{ADV}$ Low	t_{ASVL}	−5	—	ns	*2
Address Hold Time from $\overline{ADV}$ High	t_{AHV}	10	—	ns	
$\overline{ADV}$ Low Pulse Width	t_{VPL}	10	—	ns	*3
$\overline{ADV}$ Low Setup Time to CLK	t_{VSCK}	7	—	ns	*4
$\overline{CE1}$ Low Setup Time to CLK	t_{CLCK}	7	—	ns	*4
$\overline{ADV}$ Low Hold Time from CLK	t_{CKVH}	1	—	ns	*4
Burst End $\overline{ADV}$ High Hold Time from CLK	t_{VHVL}	15	—	ns	

*1: t_{ASCL} is applicable if $\overline{CE1}$ is brought to Low after $\overline{ADV}$ is brought to Low.

*2: t_{ASVL} is applicable if $\overline{ADV}$ is brought to Low after $\overline{CE1}$ is brought to Low.

*3: t_{VPL} is specified from the falling edge of either $\overline{CE1}$ or $\overline{ADV}$ whichever comes late.

*4: Applicable to the 1st valid clock edge.

22

NTC0097707

MB82DBS02163C-70L

(5) Synchronous Read Operation (Burst mode)

(At recommended operating conditions unless otherwise noted)

Parameter		Symbol	Value		Unit	Notes
			Min	Max		
Burst Read Cycle Time		t_{RC8}	—	8000	ns	
CLK Access Time		t_{AC}	—	12	ns	*1
Output Hold Time from CLK		t_{CKQX}	3	—	ns	*1
$\overline{CE}1$ Low to $\overline{WAIT}$ Low		t_{CLTL}	5	20	ns	*1
$\overline{OE}$ Low to $\overline{WAIT}$ Low		t_{OLTL}	0	20	ns	*1, *2
CLK to $\overline{WAIT}$ Valid Time		t_{CKTV}	—	12	ns	*1, *3
$\overline{WAIT}$ Valid Hold Time from CLK		t_{CKTX}	3	—	ns	*1
$\overline{CE}1$ Low to Output Low-Z		t_{CLZ}	5	—	ns	*4
$\overline{OE}$ Low to Output Low-Z		t_{OLZ}	10	—	ns	*4
$\overline{LB}$, $\overline{UB}$ Low to Output Low-Z		t_{BLZ}	0	—	ns	*4
$\overline{CE}1$ High to Output High-Z		t_{CHZ}	—	14	ns	*1
$\overline{OE}$ High to Output High-Z		t_{OHZ}	—	14	ns	*1
$\overline{LB}$, $\overline{UB}$ High to Output High-Z		t_{BHZ}	—	14	ns	*1
$\overline{CE}1$ High to $\overline{WAIT}$ High-Z		t_{CHTZ}	—	20	ns	*1
$\overline{OE}$ High to $\overline{WAIT}$ High-Z		t_{OHTZ}	—	20	ns	*1
$\overline{OE}$ Low Setup Time to 1st Data-output		t_{OLQ}	30	—	ns	
$\overline{LB}$, $\overline{UB}$ Setup Time to 1st Data-output		t_{BLQ}	30	—	ns	*5
$\overline{OE}$ Setup Time to CLK		t_{OSCK}	6	—	ns	
$\overline{OE}$ Hold Time from CLK		t_{CKOH}	5	—	ns	
Burst End $\overline{CE}1$ Low Hold Time from CLK		t_{CKCLH}	5	—	ns	
Burst End $\overline{LB}$, $\overline{UB}$ Hold Time from CLK		t_{CKBH}	5	—	ns	
Burst Terminate Recovery Time	BL = 8, 16	t_{TRB}	30	—	ns	*6
	BL = Continuous		70	—	ns	*6

*1: The output load 50 pF with 50 Ω termination to $V_{DD} \times 0.5$ V.

*2: $\overline{WAIT}$ drives High at the beginning depending on $\overline{OE}$ falling edge timing.

*3: t_{CKTV} is guaranteed after t_{OLTL} (Max) from $\overline{OE}$ falling edge and t_{OSCK} must be satisfied.

*4: The output load 5 pF without any other load.

*5: Once $\overline{LB}$ and $\overline{UB}$ are determined, they must not be changed until the end of burst read.

*6: Defined from the Low to High transition of $\overline{CE}1$ to the High to Low transition of either $\overline{ADV}$ or $\overline{CE}1$ whichever occurs late.

23

NTC0097708

MB82DBS02163C-70L

(6) Synchronous Write Operation (Burst mode)

(At recommended operating conditions unless otherwise noted)

Parameter		Symbol	Value		Unit	Notes
			Min	Max		
Burst Write Cycle Time		t_{WCB}	—	8000	ns	
Data Setup Time to CLK		t_{DSCK}	7	—	ns	
Data Hold Time from CLK		t_{DHCK}	3	—	ns	
$\overline{WE}$ Low Setup Time to 1st Data Input		t_{WLD}	30	—	ns	
$\overline{LB}$, $\overline{UB}$ Setup Time for Write		t_{BS}	-5	—	ns	*1
$\overline{WE}$ Setup Time to CLK		t_{WSCK}	5	—	ns	
$\overline{WE}$ Hold Time from CLK		t_{CKWH}	5	—	ns	
$\overline{CE1}$ Low to $\overline{WAIT}$ High		t_{CLTH}	5	20	ns	*2
$\overline{WE}$ Low to $\overline{WAIT}$ High		t_{WLTH}	0	20	ns	*2
$\overline{CE1}$ High to $\overline{WAIT}$ High-Z		t_{CHTZ}	—	20	ns	*2
$\overline{WE}$ High to $\overline{WAIT}$ High-Z		t_{WHTZ}	—	20	ns	*2
Burst End $\overline{CE1}$ Low Hold Time from CLK		t_{CKCLH}	5	—	ns	
Burst End $\overline{CE1}$ High Setup Time to next CLK		t_{CHCK}	5	—	ns	
Burst End $\overline{LB}$, $\overline{UB}$ Hold Time from CLK		t_{CKBH}	5	—	ns	
Burst Write Recovery Time		t_{WRB}	30	—	ns	*3
Burst Terminate Recovery Time	BL = 8, 16	t_{TRB}	30	—	ns	*4
	BL = Continuous		70	—	ns	*4

*1: Defined from the valid input edge to the High to Low transition of either $\overline{ADV}$, $\overline{CE1}$, or $\overline{WE}$, whichever occurs last. And once $\overline{LB}$, $\overline{UB}$ are determined, $\overline{LB}$, $\overline{UB}$ must not be changed until the end of burst write.

*2: The output load 50 pF with 50 Ω termination to $V_{DD} \times 0.5$ V.

*3: Defined from the valid clock edge where last data-input being latched at the end of burst write to the High to Low transition of either $\overline{ADV}$ or $\overline{CE1}$ whichever occurs late for the next access.

*4: Defined from the Low to High transition of $\overline{CE1}$ to the High to Low transition of either $\overline{ADV}$ or $\overline{CE1}$ whichever occurs late for the next access.

24

NTC0097709

MB82DBS02163C-70L

(7) Power Down Parameters

(At recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
CE2 Low Setup Time for Power Down Entry	t_{C2P}	20	—	ns	
CE2 Low Hold Time after Power Down Entry	t_{C2LP}	70	—	ns	
$\overline{CE}$1 High Hold Time following CE2 High after Power Down Exit [Sleep mode only]	t_{CHH}	300	—	µs	*1
$\overline{CE}$1 High Hold Time following CE2 High after Power Down Exit [not in Sleep mode]	t_{CHHP}	70	—	ns	*2
$\overline{CE}$1 High Setup Time following CE2 High after Power Down Exit	t_{CHS}	0	—	ns	*1

*1 : Applicable also to power-up.

*2 : Applicable when 4 M-bit and 8 M-bit Partial mode is set.

(8) Other Timing Parameters

(At recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
$\overline{CE}$1 High to $\overline{OE}$ Invalid Time for Standby Entry	t_{CHOX}	10	—	ns	
$\overline{CE}$1 High to $\overline{WE}$ Invalid Time for Standby Entry	t_{CHWX}	10	—	ns	*1
CE2 Low Hold Time after Power-up	t_{C2LH}	50	—	µs	
$\overline{CE}$1 High Hold Time following CE2 High after Power-up	t_{CHH}	300	—	µs	
Input Transition Time (except for CLK)	t_T	1	25	ns	*2, *3

*1 : Some data might be written into any address location if t_{CHWX} (Min) is not satisfied.

*2 : Except for clock input transition time.

*3 : The Input Transition Time (t_T) at AC testing is 5 ns for Asynchronous operation and 3 ns for Synchronous operation respectively. If actual t_T is longer than 5 ns or 3 ns specified as AC test condition, it may violate AC specification of some timing parameters. Refer to " (9) AC Test Conditions".

25

NTC0097710

MB82DBS02163C-70L

(9) AC Test Conditions

Description		Symbol	Test Setup	Value	Unit	Notes
Input High Level		V_{IH}	—	$V_{DD} \times 0.8$	V	
Input Low Level		V_{IL}	—	$V_{DD} \times 0.2$	V	
Input Timing Measurement Level		V_{REF}	—	$V_{DD} \times 0.5$	V	
Input Transition Time	Async.	t_T	Between V_{IL} and V_{IH}	5	ns	
	Sync.			3	ns	

• AC MEASUREMENT OUTPUT LOAD CIRCUIT

26
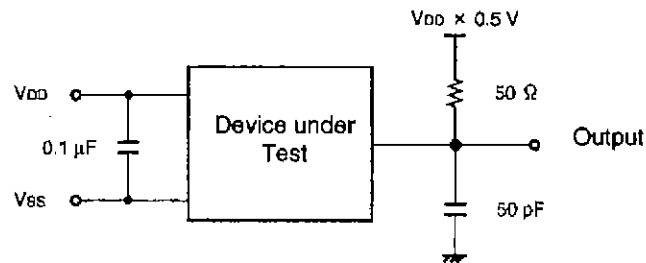
■ TIMING DIAGRAMS

(1) Asynchronous Read Timing #1-1 (Basic Timing)

Note : This timing diagram assumes CE2 = H and $\overline{WE}$ = H.

27

NTC0097712
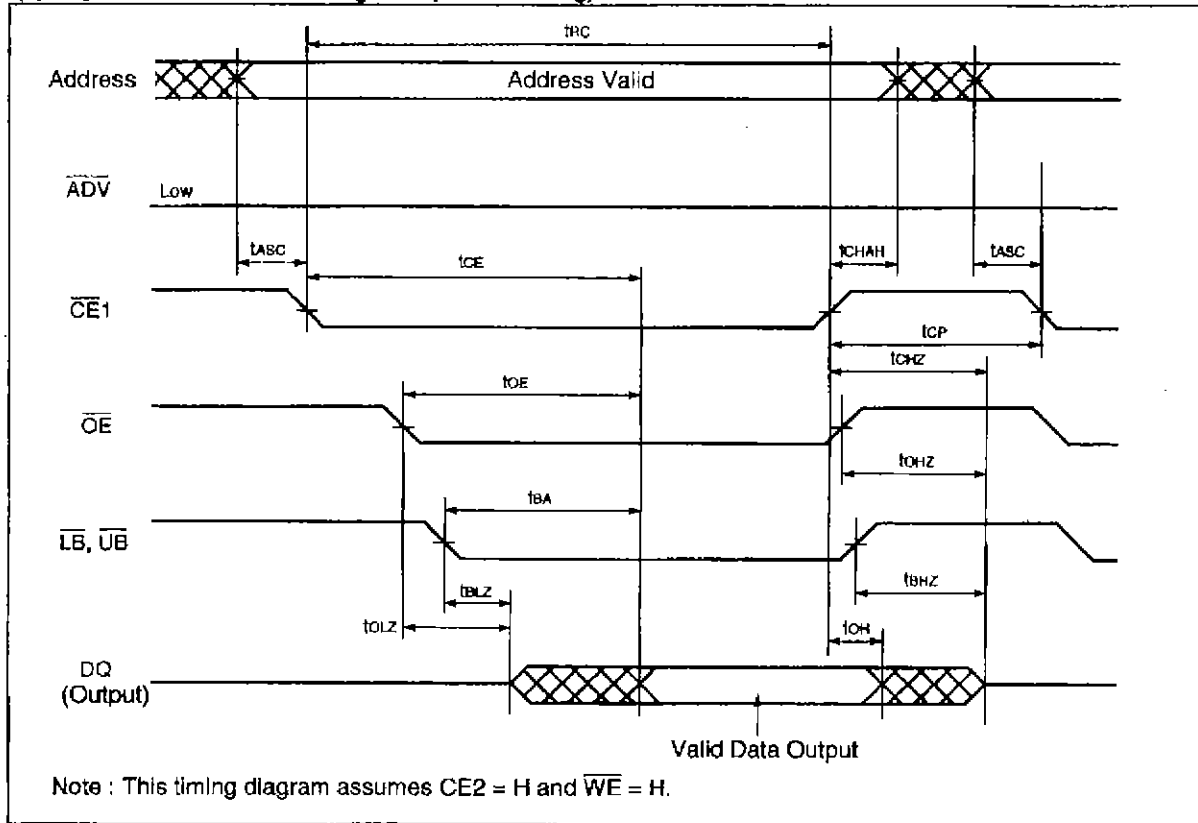
MB82DBS02163C-70L

(2) Asynchronous Read Timing #1-2 (Basic Timing)

Note : This timing diagram assumes CE2 = H and $\overline{WE}$ = H.
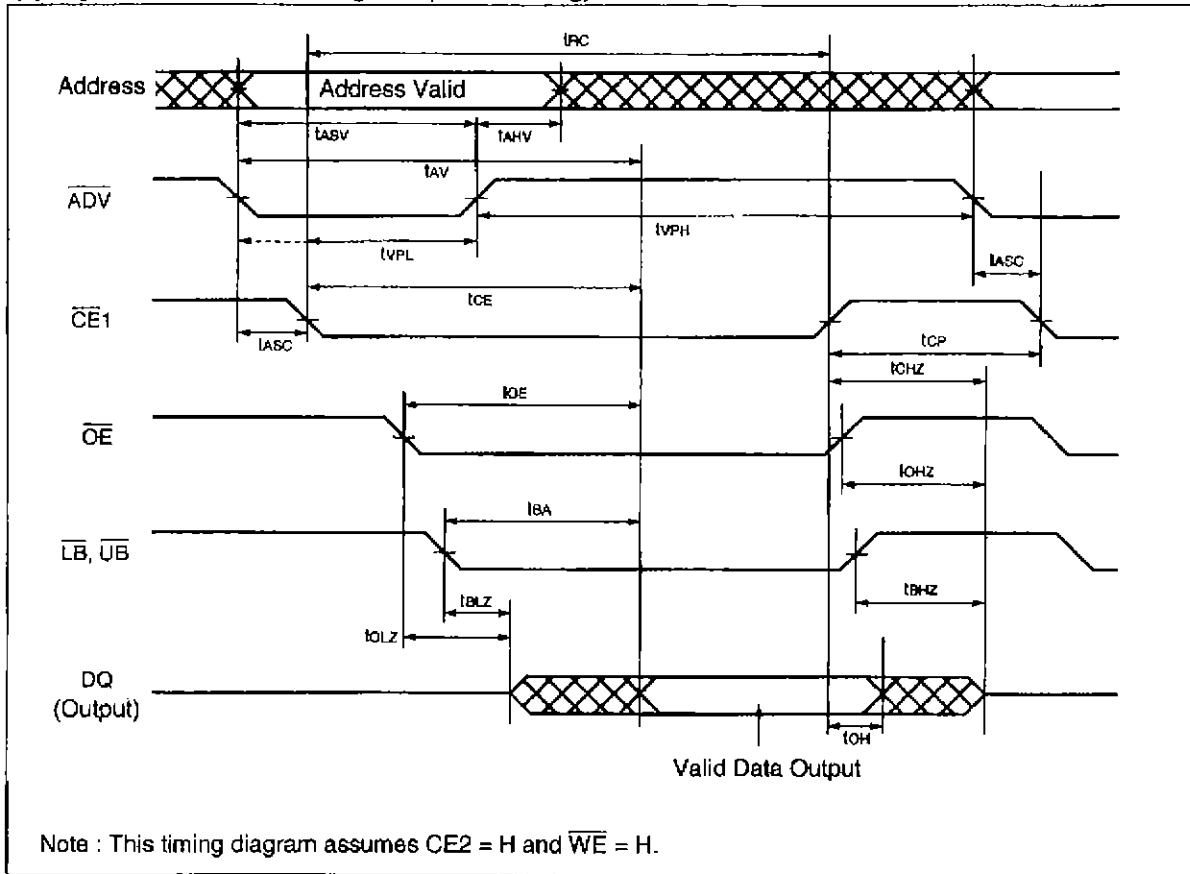
MB82DBS02163C-70L

(3) Asynchronous Read Timing #2 (OE Control & Address Access)

Note : This timing diagram assumes CE2 = H, ADV = L and WE = H.

29
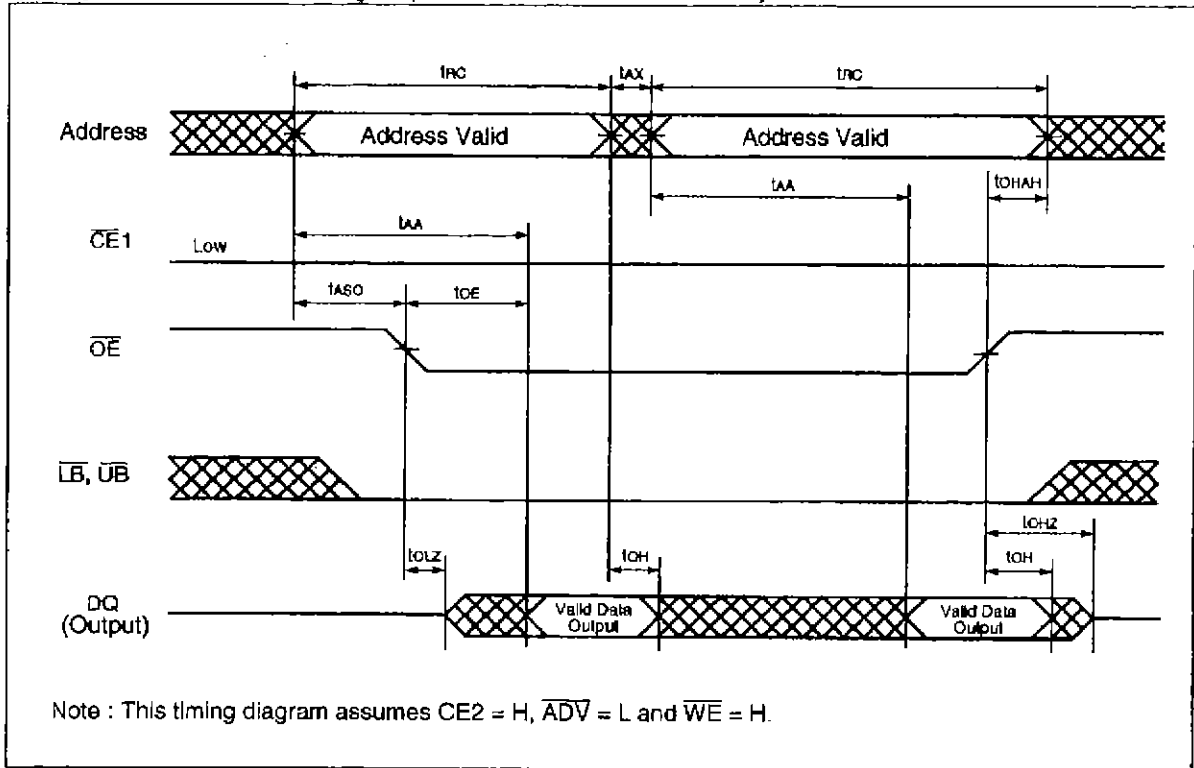
MB82DBS02163C-70L

(4) Asynchronous Read Timing #3 ($\overline{LB}$, $\overline{UB}$ Byte Control Access)

Note : This timing diagram assumes CE2 = H, $\overline{ADV}$ = L and $\overline{WE}$ = H.

30